LONUSERS® INTERNATIONAL

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Troubleshooting LONWORKS® Devices and Twisted Pair Networks

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[1] Introduction

[1.1] Scope & Audience

- This tutorial paper covers the troubleshooting of Neuron® Chip-based devices, from the Neuron chip circuitry, through the transceiver and out onto the network. It is targeted at engineers and technicians that are developing LONWORKS® devices in the lab, as well as field service personnel that are troubleshooting network installations in the field.

- This paper does not cover power line communication networks. For good information on troubleshooting power line networks, see the *PLT-10/20/21/30 Power LineTransceiver User's Guides*, and the *PLCA, PLCA-20/21/30 Power Line Communications Analyzer User's Guides*.

- This paper assumes that the audience is already familiar with the basic concepts of LONWORKS, including the LONWORKS protocol, protocol analysis tools, and network wiring & terminations. A working knowledge of test tools (oscilloscopes, logic analyzers, etc.) is also assumed.

[1.2] Revision History

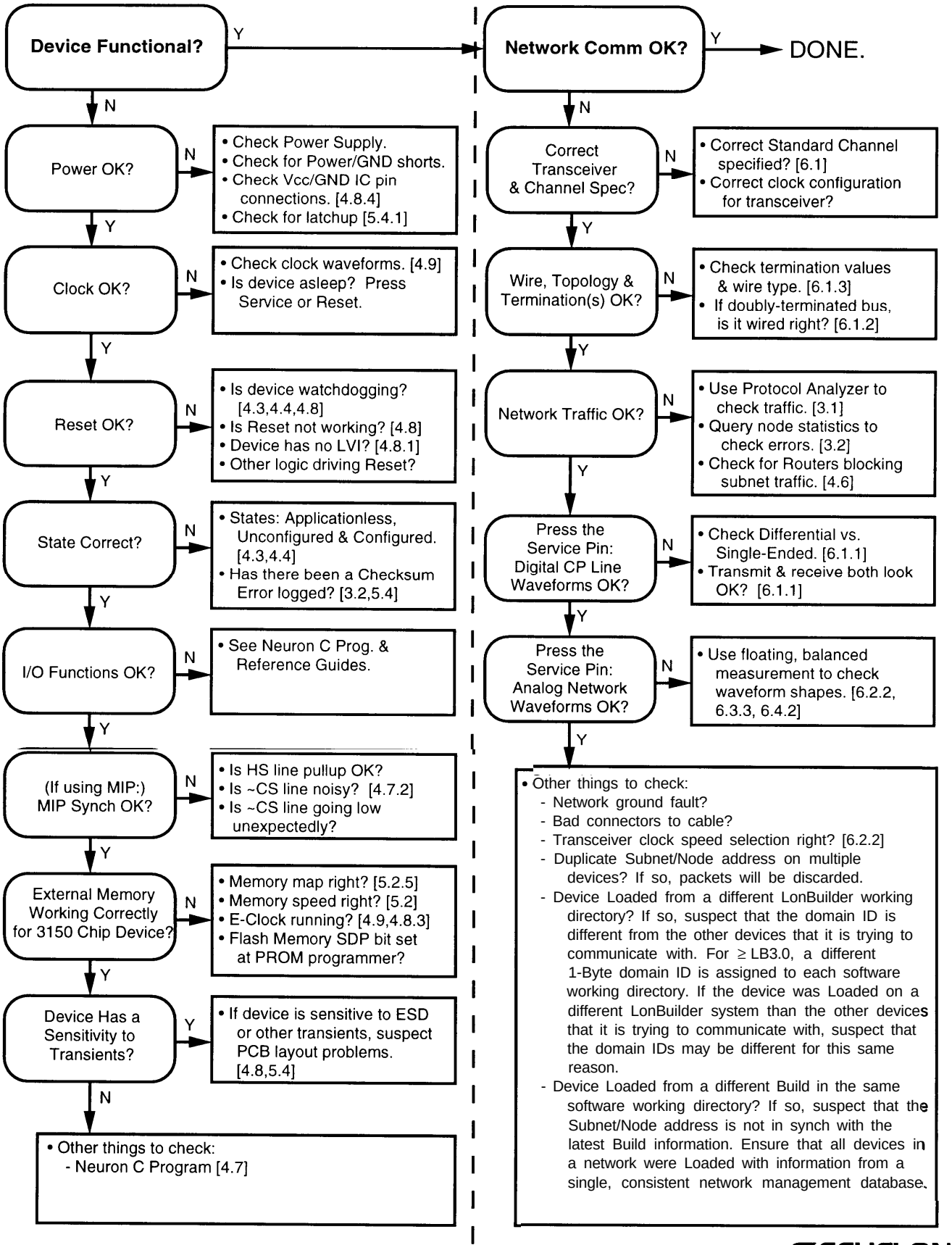
- The first revision of this tutorial paper was given at the LONUSERS® International Conference in May, 1996, in Santa Clara, California.

- An updated revision of the paper was given at the LONUSERS International Conference in October, 1996, in Nice France. The organization of the paper was changed somewhat, several typographical errors were fixed, and a few more troubleshooting tips were added.

- This latest revision fixes one typographical error -- on page 23, the Service LED behavior for EEBlank from LonBuilder 3.0 has been corrected.

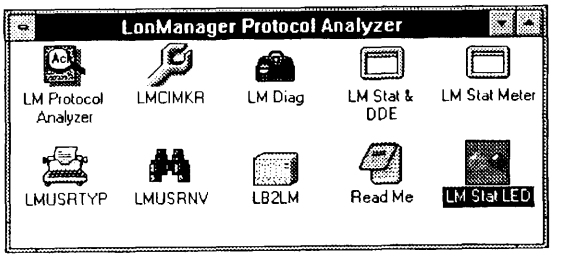
- For extra copies of this troubleshooting paper, send e-mail to berke@echelon.com, or check Echelon's website.[16] Readers of this paper are encouraged to send information on their own troubleshooting tips to Echelon for incorporation into future revisions of this paper. Please send your tips to the e-mail address listed above.

[2.] Troubleshooting Strategy Flowchart



[3.] Troubleshooting Tools

[3.1] Protocol Analysis Tools



[3.1.1] LonManager® Protocol Analyzer[9]

- Hardware:
  PCC-1O Protocol Analyzer card (PCMCIA Type II card)
  LMPA card (Full-size ISA bus card)

- Software:
  LMCIMKR: Use to create channel definitions

  LB2LM: Use to convert LonBuilder databases to LonManager DB format

  Protocol Analyzer: Main application for gathering packet information into tabular format. The number of packets logged is limited only by the size of the PC's disk. Filters can be used to selectively log packets

  Statistics: This application summarizes statistical info about the network traffic, including good & bad packet summaries.

  Diagnostics: Using a LonManager DB for information about a node's network address, the Diagnostics application lets you manipulate the node (P ing, S tatus, Of f Line, O n Line, R eset, C l ear, W ink).

[3.1.2] LonBuilder® Protocol Analyzer[10]

- Hardware: LonBuilder Development Station (limited to lab use, generally)

. Software: Protocol Analyzer, Statistics, some Diagnostics

[3.] Troubleshooting Tools (cont.)

[3.2] Other Test Software

[3.2.1] LonBuilder & NodeBuilder Development Tools

- Use Install, Test, Wink, Query, etc. to debug devices

[3.2.2] LonMaker™ & Other API/ LNS Based Network Management Tools

- Install, Test, Wink, and other commands are generally available

[3.2.3] NodeUtil

- Shareware DOS/Windows program (available at Echelon's FTP site)
  - Press the Service Pin on a device to temporarily register it
  - Once Nodeutil has registered a node, commands can be used to interrogate & manipulate the node. Find nodes, change node Mode, Reboot node, report Status and Goto node menu are the most commonly used commands.
  - No database is kept by NodeUtil . . ..all device information is lost when the program exits.
  - . USE NodeUtil WITH CARE!! Changes made to a device's configuration during debugging can confuse the network management software responsible for the device. Use the network management software for debug whenever possible.

Run NodeUtil to Get the Main Menu:

```
C: \WINDOWS>nodeutil
Node Utility Release 1.31
Copyright (c) 1995 Echelon Corporation.  All rights
reserved.
Successfully installed network interface.
Welcome to the LONWORKS Node Utility application.
Activate the service pin on remote node to access it .
Enter one of the following commands by typing the indicated
letter :

A -- (A)dd node to list,
c -- Set (c) lock rates of the network interface.
D -- Set the (D) omain of the network interface
E -- (E)xit this application and return to DOS .
F -- (F) ind nodes in the current domain.
G-- (G)oto node menu..... . . . . . .
H -- (H)elp with commands
L -- Display node (L)ist.
M -- Change node (M) ode or state.
O -- Redirect (0)utput to a file.
P -- Send a service (P)in message from a PCLTA
R -- (R)eboot 3150 node.
S -- Report node (S)tatus and statistics.
V -- Control (V)erbose modes
W -- (W) ink a node.
Z -- Shell out to DOS.
NODEUTIL>
```

Then Press Service Pin on a Device:

```
NODEUTIL> Received an ID message from node 1.
Program ID is SVCPONG2
NODEUTIL>
```

"G1" To Goto Node #l Menu:

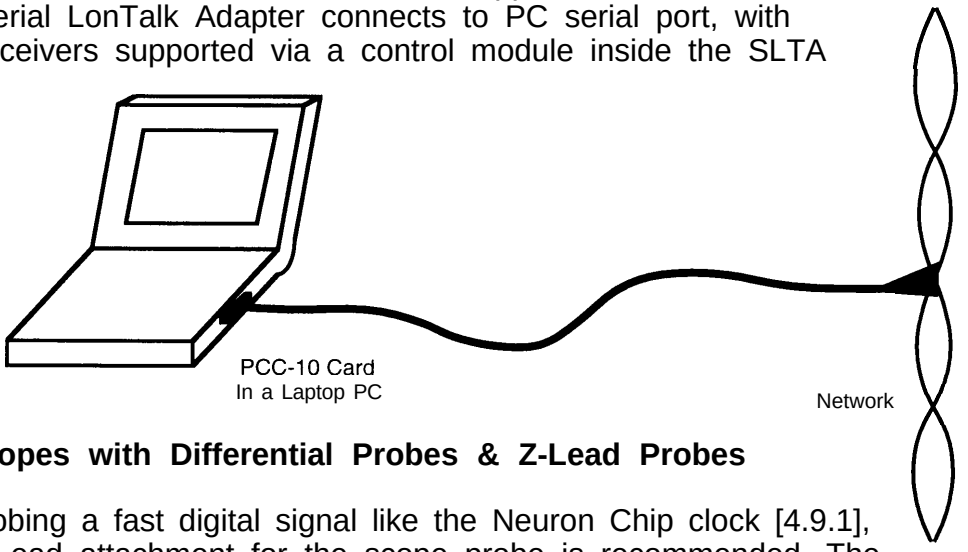
```
Enter one of the following commands:
A -- Node (A)ddress table.
B --  (B)uffer configuration.
c -- Application (C)onfiguration structures.
D -- Node (D)omain table.
E --  (E)xit this menu and return to main menu.
G --  (G)o to another node.
H --  (H)elp with node commands.
1 -- Network variable al(I)as table.
J --  (J)am network variable type.
L --  (L)ist network variables.
M -- Change node (M)ode or state.
N --  (N)etwork Variable configuration table.
0 -- Redirect (0)utput to a file.
P --  (P)oll network variable.
R --  (R)ead node memory.
s -- Report node (S)tatus and statistics.
T --  (Transceiver parameters.
u --  (U)pdate input network variable.
v -- Control (V)erbose modes.
w --  (W)rite node memory.
x -- Create eternal interface file.
NODE :1>
```

[3.] Troubleshooting Tools (cont.)

[3.3] Test Hardware

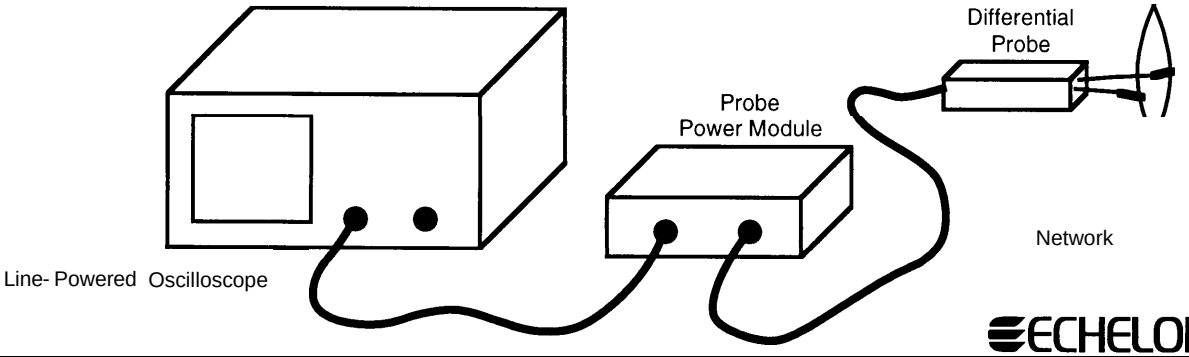
[3.3.1] Network Interfaces

- PCC-1O: PCMCIA Type II card with FTT-1OA on-board, other transceivers are supported via external cable "pods"
- PCLTA-1O: Half-Length, Half-Height, Plug and Play lSA-bus card with either FTT-1O, TP/XF-78 or TP/XF-1250 transceiver on-board
- PCLTA: lSA-bus card with transceivers supported via SMX transceivers
- SLTA: Serial LonTalk Adapter connects to PC serial port, with transceivers supported via a control module inside the SLTA



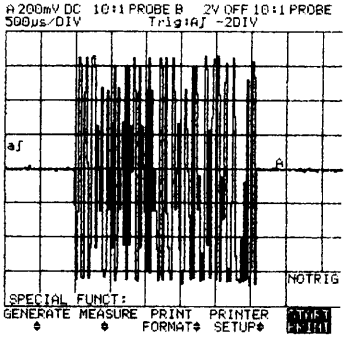
[3.3.2] Oscilloscopes with Differential Probes & Z-Lead Probes

- When probing a fast digital signal like the Neuron Chip clock [4.9.1], a Z-Lead attachment for the scope probe is recommended. The Z-Lead probe allows less inductance in the probe's ground line, and allows monitoring the clock signal without introducing false ringing.
- When using a line-powered oscilloscope to monitor analog waveforms on a real-world network, a differential probe must be used to accommodate the network's common mode voltage noise, and to avoid introducing imbalances into the network. Before making a signal measurement on the network, check that a quiet OV signal is displayed on the scope when both differential probes are connected to the same wire in the twisted pair (either wire). This ensures that the differential probe is correctly balanced.
  Two common differential probes used by Echelon are:
  - HP 1141A Differential Probe (using xl O attenuator head) with HP1142A Power Module
  - Tektronix P6046 Differential Probe (using xl O attenuator head) with Amplifier and Power Supply

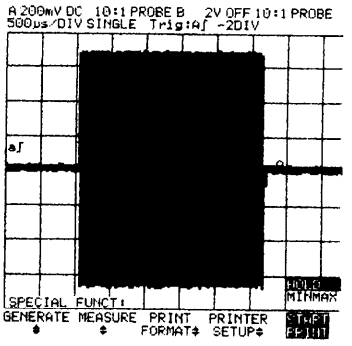


[3.3.3] Battery-Powered Portable Oscilloscopes

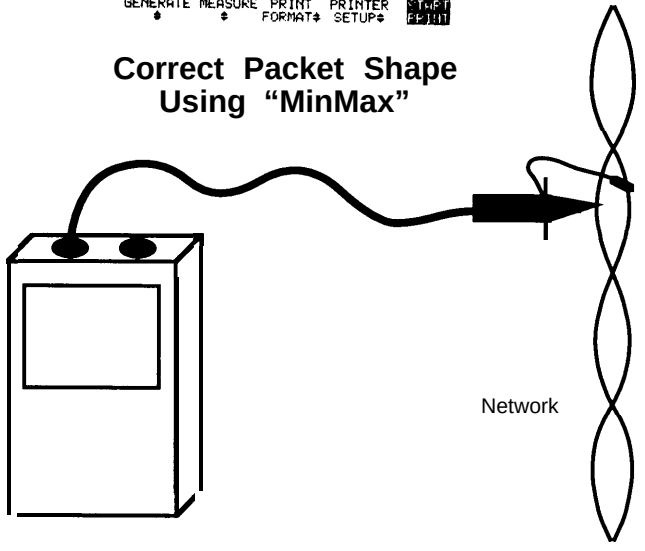
- Small, battery-powered oscilloscopes are an alternative to line-powered oscilloscopes with differential probes. The battery-powered scope's probe can generally be connected directly across the network wire pair. (Do not connect the scope's second probe to anything.) Before making a signal measurement on the network, check that a quiet OV signal is displayed on the portable scope when both the probe and its ground lead are connected to the same wire in the twisted pair (either wire). This ensures that the scope is floating sufficiently well to make a valid differential measurement.
- The analog waveforms shown in section 6 of this Troubleshooting Guide were obtained using a Fluke ScopeMeter 97 (50 MHz battery-powered oscilloscope). Note that the ScopeMeter 97 shows the shape of a packet best when MinMax is used on Channel A:



Undersampled Packet Shape Without "MinMax"



Correct Packet Shape Using "MinMax"



Portable, Battery-Powered Oscilloscope

Network

[3.3.4] Logic Analyzers

. A logic analyzer can be helpful for checking the basic execution of Neuron 3150 Chip devices when external memory problems are suspected [5.2.4].

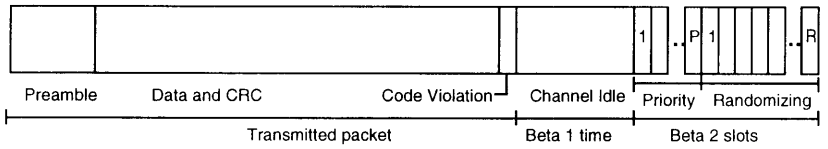
. Some means of connecting the logic analyzer probes into the memory circuit must be used. Echelon has used the Bug Katcher™ series from Emulation Technology (ET part number BC4-32-PCC7-OOO0 can be used to monitor memory bus execution from a 32-pin PLCC PROM socket).

[4.] Overall Concepts

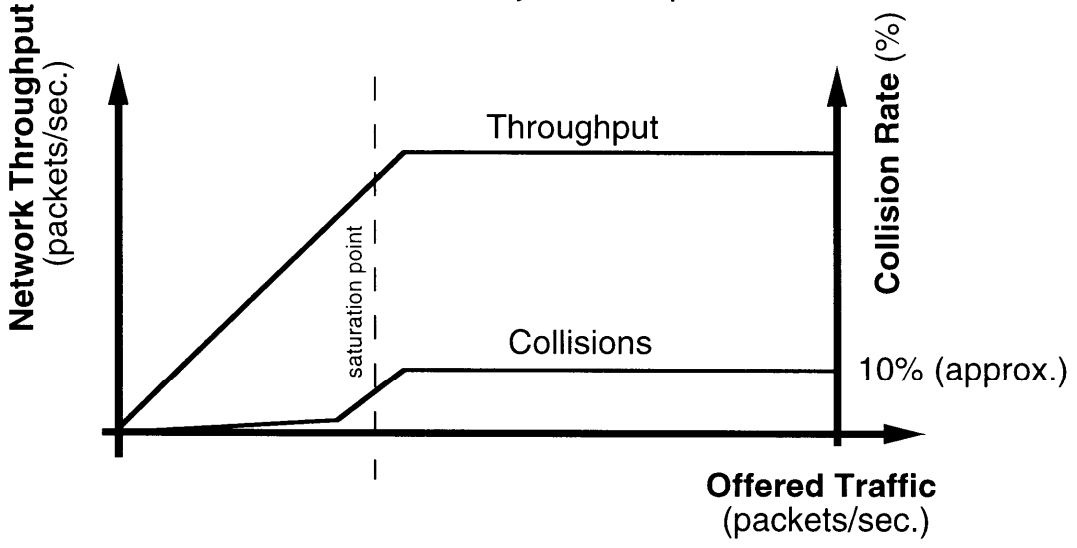
[4.1] LONWORKS Networks, p-CSMA and CRC Errors

- **LONWORKS networks use a patented technique called p-CSMA[1,14,15] (p-persistent, carrier Sense, Multiple Access) for managing packet access to the network. p-CSMA allows the throughput of a saturated network to remain high, and allows the collision rate to remain low.**

  - Each transmitted packet is followed by a Beta 1 time, and some number of Beta 2 time slots. The Beta 1 time can be thought of as a "settling" time for the network. Each Beta 2 slot is wide enough so that all devices on the network will detect the start of transmission from any other device in time to avoid starting their own transmission in the next Beta 2 slot.



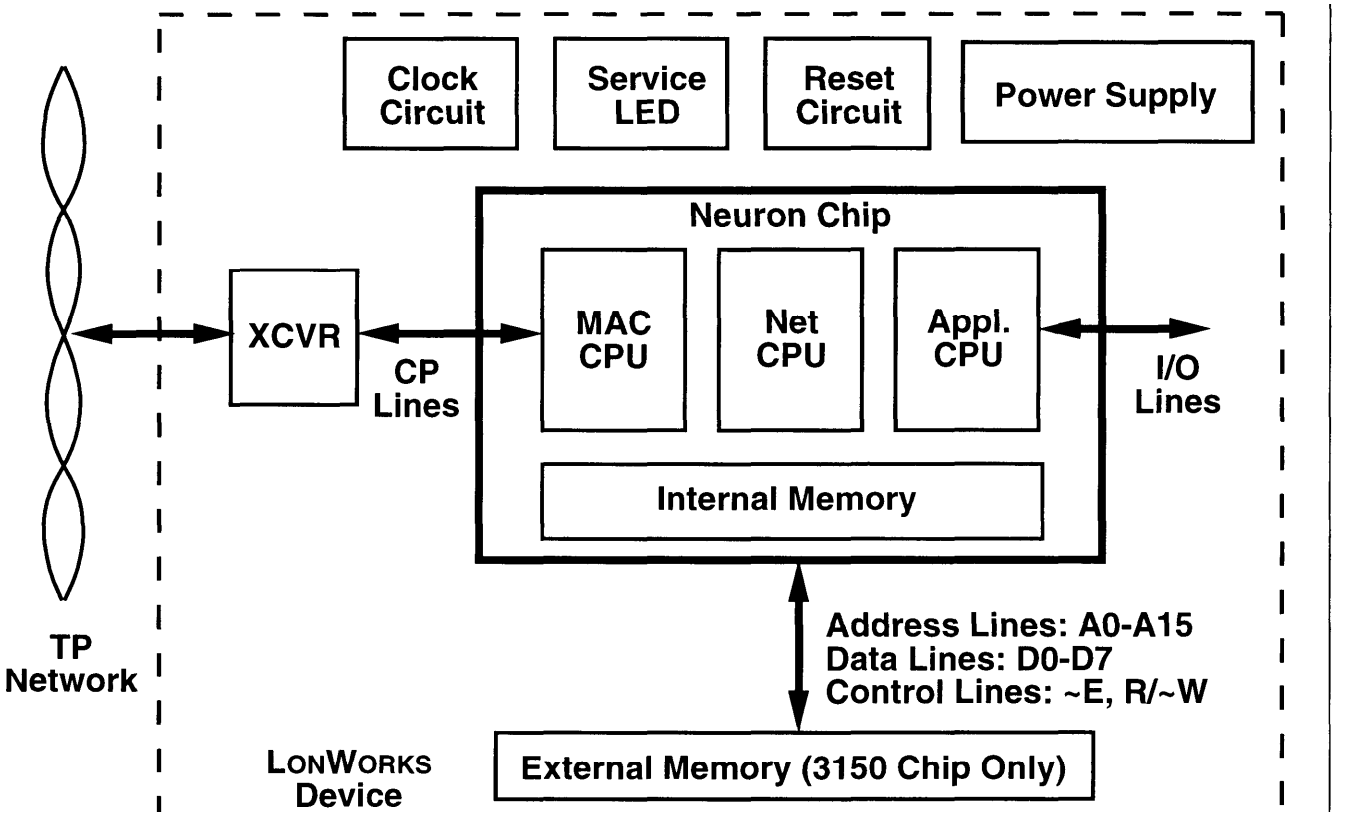
  - When a device is ready to transmit a packet, it picks a random number between 1 and R. This determines which Beta 2 slot the device will attempt transmission in during the next packet cycle. On a quiet network, R=16. On a very busy network, the p-persistent feature allows the devices to cooperate to grow the number R (up to 1008). The greater number of randomizing Beta 2 slots lowers the individual probability of a device's packet colliding with another packet, and this unique feature keeps the maximum collision rate on a saturated LONWORKS network down to just a few percent.



  - Thus, even on a saturated network (where the number of packets per second that can be "offered" to the network by the devices exceeds the channel capacity), there should not be a high collision rate. If a device is reporting a high collision rate, suspect a problem with its transceiver or the network wiring [6.1-6.5].

[4.] Overall Concepts (cont.)

[4.2] Block Diagram of a LONWORKS Device on a Twisted Pair Network:



- See the Neuron Chip databooks for a complete description of Neuron Chip operation.

- The three CPUs interleave accesses to memory for instruction execution and memory read/write operations. The Neuron 3120 Chip runs completely from internal memory, while the Neuron 3150 Chip runs from both external and internal memory. For convenience, the division of tasks among the three CPUs is described briefly here:

  - **MAC CPU:** The Media Access Control CPU is responsible for interfacing with the transceiver. It handles all physical layer transmitting and receiving of packets, including implementing the p-CSMA algorithm.

  - **Network CPU:** The Network processor manages the incoming and outgoing message buffers. It is also responsible for managing the software timers.

  - **Application CPU:** The Application processor runs the Neuron C application program. When a non-MIP device is in the Unconfigured state (see [4.3]), the Neuron C application program does not execute. A non-MIP device must be in the Configured state for the application to run.

[4.] Overall Concepts (cont.)

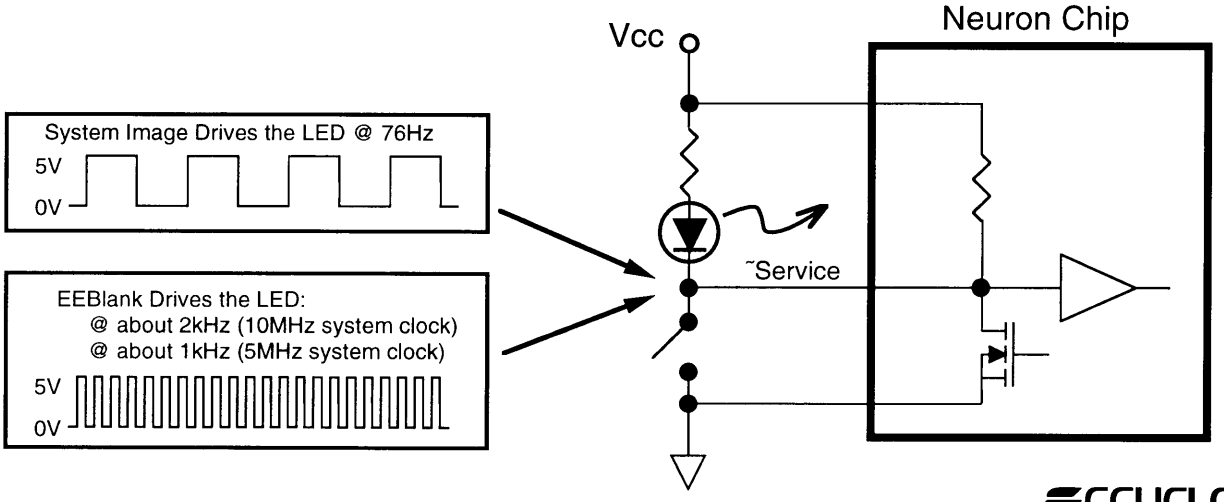
[4.3] Configuration States of a Device

- **A LONWORKS device can be in one of the following three firmware states:**
  - **Applicationless:** Only communication parameters are loaded into the device's internal EEPROM. The Service LED (see [4.4.2]) remains ON solid in the Applicationless state.
  - **Unconfigured:** In addition to its communication parameters, the device contains an application program. The Service LED blinks at a 1/2 Hz rate in the Unconfigured state. The device does not yet have information about its network configuration (like its network address, network variable binding information, etc.). A non-MIP device does not execute its Neuron C application program while it remains in the Unconfigured state. A MIP device does execute its MIP application when in the Unconfigured state, so that it can communicate with the MIP's host processor.
  - **Configured:** In addition to the information from the Unconfigured state, a Configured device has been assigned its network addresses and binding information. The Service LED is generally OFF in the Configured state, and the Neuron C application program is running.

[4.4] Service LED Behavior

[4.4.1] Service Pin Drive Waveforms[1]

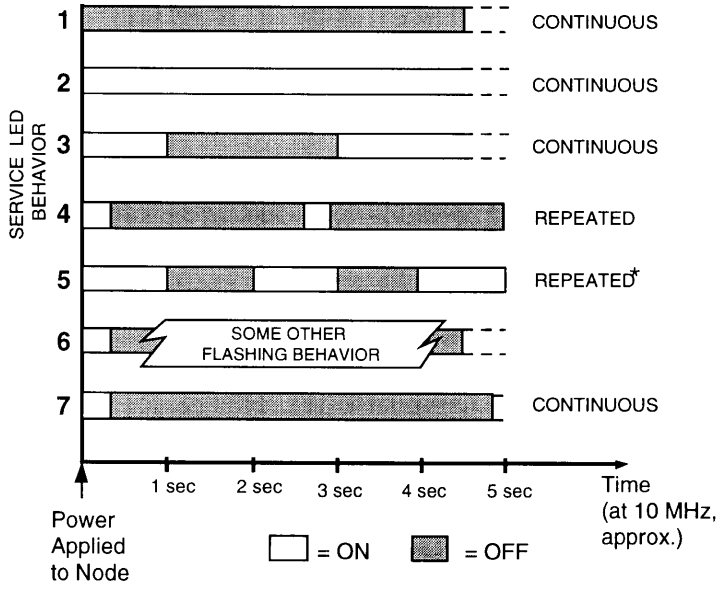
- Service Pin is used to drive the Service LED & to read the Service Switch state:
  LED Off: -Service = 5V
  LED On: -Service = square wave drive waveform (see below)
  Service Switch Pressed: -Service = Ground



[4.4] Service LED Behavior (cont.)

[4.4.2] Service LED Flashing Behaviors[11]

- (See the next slide for an explanation of these flashing behaviors)



*Does not scale with the Neuron Chip clock

[4.4.2] Service LED Flashing Behaviors (cont.)

Flashing Behavior & Context	Likely Explanation
1: LED is OFF continuously as soon as power is applied to device.	• Bad device hardware. Suspect power supply problems [4.8.4], clock problems [4.9], or a bad Neuron Chip.
2: LED is ON continuously, even when power is first applied to the device.	• Bad device hardware. Suspect power supply problems [4.8.4], clock problems [4.9] or a bad Neuron Chip. For a 3150 Chip device, also check for a short between pin 17 (-Service) and pin 18 (Do Not Connect). Pin 18 is an output that toggles during execution, and this fault can cause a continuous stream of Service Pin packets to be sent.
3: LED flashes at power-up, goes OFF, then comes ON solid.	• This is the normal behavior for an Applicationless device [4.3]. If the device is not supposed to be Applicationless, suspect a checksum error caused by LVI problems [4.8.1], memory problems [5.2], PCB layout problems [5.4], or application code errors. A self-test failure can also turn the LED ON solid.
4: LED flashes briefly once every second for a 10MHZ device, or once every two seconds for a 5MHz device.	• This device is probably experiencing continuous Watchdog resets. For a Neuron 3120 Chip device, suspect bad application code (i.e., "scheduler bypass" code that does not update the Watchdog timer), or a bad Neuron Chip. for a Neuron 3150 Chip, additionally suspect the integrity of the external memory design & connections [5.2].
5: LED blinks ON & OFF at l/2Hz rate,	• This is the normal behavior for an Unconfigured device [4.3]. If the device is not supposed to be Unconfigured, suspect a checksum error caused by LVI problems [4.8.1], memory problems [5.2], PCB layout problems [5.4], or application code errors.
6: When using EEBlank, ...	• The flashing behavior of the Service LED indicates the progress of the EEBlank procedure [5.2.3]. This behavior depends on device clock speed, and on the version of EEBlank.NRI (the behavior changed for ≥ LB3.0).
6: At the first power-up of a Neuron 3150 Chip device with a new PROM	• If the new PROM was exported Applicationless, the LED will flash ON briefly at the application of power, then will turn OFF for about 1 second, and then will turn ON and stay ON, • If the new PROM was exported Unconfigured, the LED will flash ON briefly at the application of power, then will stay OFF for about 1-15 seconds, depending on the size of the application code and the device clock speed. At the end of this 1-15 seconds, the LED should begin flashing with behavior #5, which indicates the Unconfigured state. • If the new PROM was exported Configured, the LED will flash ON briefly at the application of power, then will stay off for an indefinite period of time (indicating that the Neuron chip is in the Configured state).
While the LED is ON, its brightness seems to visibly flicker at about 10-30HZ.	• When the standard Neuron Chip Firmware turns on the Service LED, it uses a square wave at 76Hz to drive the LED circuit [4.4.1]. This 76Hz frequency is high enough to make the LED appear to the eye as if it is solid ON, However, if the Neuron Chip has an incorrect clock configuration in its EEPROM memory, it can incorrectly drive a lower frequency square wave when turning on the LED. For example, if the Service pin waveform is a square wave at 38 Hz, then suspect that a 5MHz device has been loaded with an image built for a 10MHz device. Similarly, if the frequency of the Service pin waveform is 152Hz, suspect that a 10MHz device has been loaded with an image built for a 5MHz device.

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[4.5] The Different Effects of "Installation"

[4.5.1] LonBuilder Tool Installation of Devices

- The LonBuilder tool is unique, because its installation of devices is "passive"
  - When a device is installed by the LonBuilder software, the Service Pin message is received by the LonBuilder tool, and the device's Neuron ID & Program ID are recorded in the LonBuilder database.
  - No return messages are sent from the LonBuilder software to the device during this installation. Thus, as long as a device can transmit its Service Pin packet, it can successfully be installed under LonBuilder software. If the device cannot receive packets, this is not apparent until other communication is attempted with the device (i.e. through a "Test" or "Load/Start").

[4.5.2] API-Based Network Management Tool Installation of Devices

- API-Based Network Management tools have an "active" installation process
  - After receiving a device's ID information, API-based tools communicate further with the device to update location & configuration information. Thus, a device must be able to both transmit & receive in order to be successfully installed with an API-based tool.
  - API-based tools include LonMaker and Node Builder from Echelon, as well as ICELAN-G™, DragNet™ and MetraVision™ from other vendors.

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[4.6] Router Issues

[4.6.1] Router Installation[8]

- A LONWORKS Router contains two Neuron Chips that communicate with each other via their I/0 lines. Each Neuron Chip has its own transceiver connected to a separate segment of the network. Each Neuron Chip in the Router has its own Domain/Subnet/Node address, in order for it to be able to communicate with the network. In order to configure the Router with its addresses, it must be installed with a Network Management Tool.

[4.6.2] Common Router Problems

SYMPTOM	POSSIBLE CAUSE
Performing a Load/Start of a device through a Router fails, and the Router stops working afterwards.	• The network management tool that is being used to do the Load/Start does not have the correct Subnet/Node ID information for the two Router halves. One of the Router IDs may match the device that is being loaded, and the Load/Start is affecting the configuration of the Router too.
A device can be Installed through a Router using a LonBuilder Tool, but other communication with the device fails.	• The device may have a faulty receiver [4.5,6.1]. • The device may already be in the Configured state, with a Subnet ID that is being blocked by the Router. Service Pin packets are not blocked by Routers. It is generally best to avoid installing pre-Configured devices on networks that contain Routers, unless the Subnet ID matches the target Subnet already.

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[4.7] Other General Neuron Chip Operation Issues

[4.7.1] Multiprocessor Issues: MAC, Network & Application Processors

- The three processors in the Neuron Chip must be able to work together in order for the device to function correctly (see [3.2]):

SYMPTOM	POSSIBLE CAUSE
Device experiences strange communication buffer problems	• Check to see if the application program is testing a msec timer in the body of the code, instead of using a when(timer_expires) clause. The Network Processor normally manages the timers, and posts expiration events for notification of the Application Processor. However, if the Application Processor directly checks the timers, the Network Processor gets slowed down by this interference, and its normal communication buffer processing job may be compromised. Avoid directly checking msec timers,

[4.7.2] MIP Issues

- See the Microprocessor Interface Program (MIP) User's Guide for a thorough discussion of issues. Here are some common problems:

SYMPTOM	POSSIBLE CAUSE
Synchronization between the master and slave is lost intermittently	• The handshake (HS) line may be glitching, or may have excessive noise. Ensure that there is a pullup resistor on this active low signal (see the MIP User's Guide). • The chip select (~CS) line may be glitching, or may have excessive noise. Use a Z-lead oscilloscope probe to check the analog waveform to ensure that it is clean. If the host processor tri-states the ~CS line during its reset period, add a pullup resistor to the ~CS line to keep it inactive during host resets. Avoid long cables between the Neuron Chip and the MIP host processor.

[4.7.3] Other Issues*

- Neuron C code problems are beyond the scope of this paper, but here are some common problems:

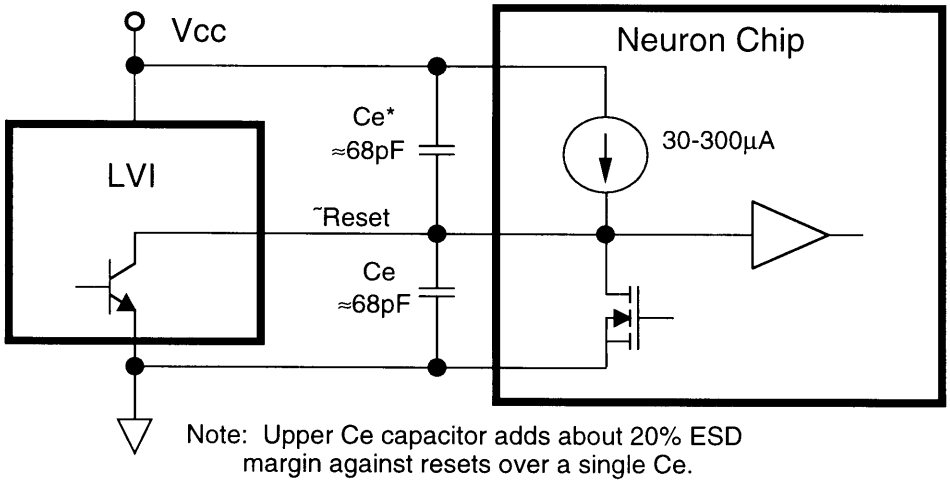
SYMPTOM	POSSIBLE CAUSE
A software timer occasionally "just stops"	• Check to see if a random function is being used to randomize the value of the timer. Remember that the random() function returns 0..255, and that assigning O to a timer will turn it off. When using the random() function in code, ensure that a O return value will not cause problems.
Network management communication with the device fails at the end of a Load/Start	• The delay in the device's when(reset) Neuron C code may be too long. See [4.8.4] for a further explanation.

[4.8] Reset Issues

[4.8.1] LVI Function (Required on All Devices)

- **Undervoltage Reset function is NOT optional!**
  - Neuron Chips must have a reliable LVI to prevent EEPROM corruption: LVI ("Low Voltage Interrupt/Inhibit") asserts --Reset when Vcc is low
- **The ~Reset line is a high-impedance, shared line**
  - Use Ce caps for decoupling of the 'Reset line (Ce ≤ 250pF total)
  - Keep the ~Reset line short, and guard it with ground as much as possible
  - Buffer the ~Reset line if it has to be routed off-board
  - An Open Collector or Open Drain LVI output is REQUIRED
  - If you have an existing node design with a non-open collector LVI, you must add a Schottky isolation diode (1N6263 or MMBD301LTI).
- **An LVI is a special kind of circuit:**
  - Reliable assertion of ~Reset should be guaranteed for Vcc ≥ 1.5V (the LVI must be connected directly to the Neuron Chip 'Reset pin)
  - A Pulse-Stretching LVI is needed with the FTT-10[3] or Flash memory[12]
  - Note: when using an LVI, the old diode-capacitor delay circuit on the 'Reset line is not needed
- **The Internal LVI in 2nd generation Neuron Chips (3120B1, 3150B1) can be used if:**
  - The Neuron Chip is guaranteed to start up correctly on power-up using only its internal LVI circuit (consult Motorola & Toshiba)
  - Other external circuitry can tolerate a low LVI trip point (3V-4V range) . . . . . Be sure to check vour external memory operating voltage range!'
  - A pulse-stretching LVI is not needed

MC34064
MC34164
MC33064
MC33164
DS1233-5
DS1233-10
DS1233Z-5
DS1233Z-10
(NOT DS1233A!)
(NOT DS1233D!)



Note: Upper Ce capacitor adds about 20% ESD margin against resets over a single Ce.

[4.8.2] Ce Capacitor on ~Reset Input Pin

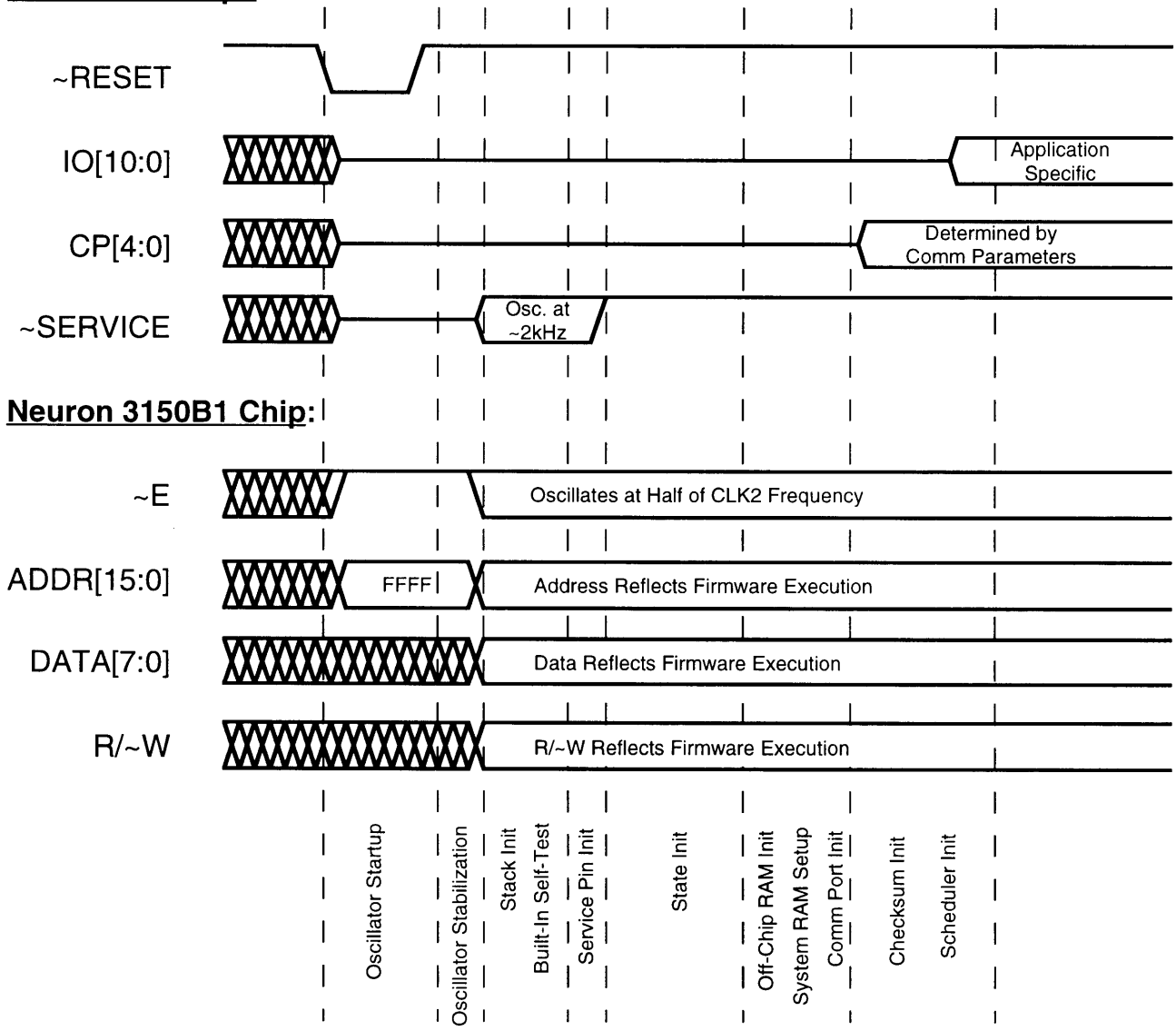
- **The Ce capacitors on the ~Reset input help reject ESD transients**
  - Place approximately 100pF on the ~Reset pin to ground. Keep the Ce capacitor as close as possible to the Neuron Chip. This capacitance holds the high-impedance ~Reset line stable during ESD hits, and thus helps prevent false resets.
  - Using two Ce capacitors split between Vcc & Ground can add about an additional 20% ESD margin over a single Ce cap.

[4.8] Reset Issues (cont.)

[4.8.3] Reset Process & Timing

- See the Neuron Chip databooks[1] for a complete discussion of the Reset process & timing issues.
- A simplified version of the Reset process timeline is shown below for convenience:

All Neuron Chips:



Neuron 3150B1 Chip:

[4.8] Reset Issues (cont.)

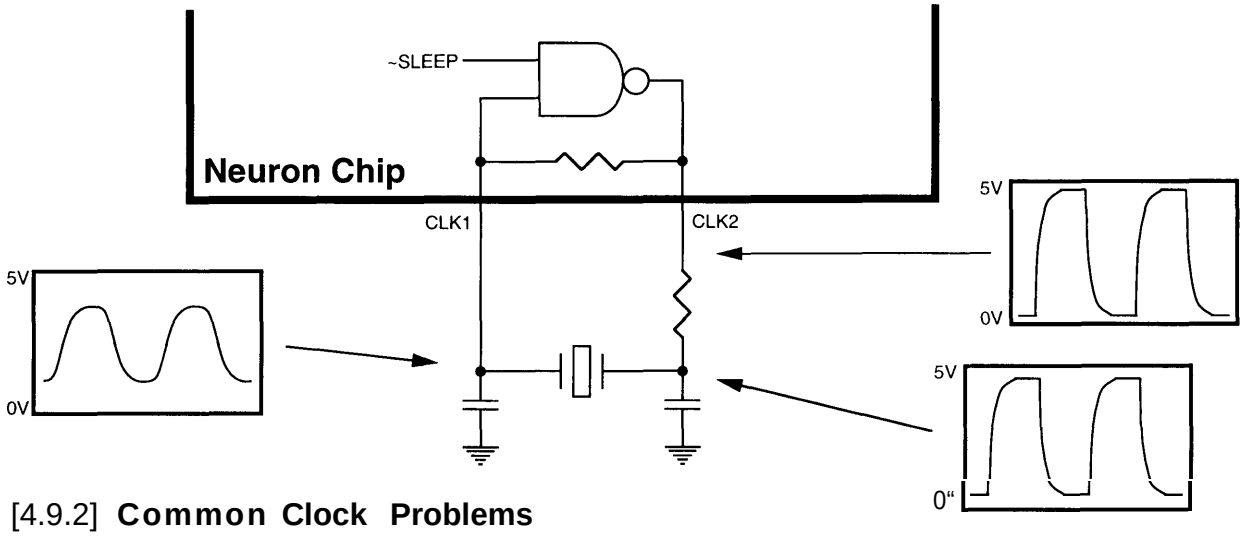
[4.8.4] Common Reset Problems

SYMPTOM	POSSIBLE CAUSE
-Reset line stuck low	• Vcc low (so LVI asserts -Reset). • No clock to B1 Neuron Chip (chip holds -Reset low).
Device resets after ESD hits	• Ce capacitor missing in reset circuit [4.8.2]. • PCB layout allows ESD current to flow through the Neuron Chip or external memory [5.4]. • Other circuitry that can drive -Reset may be glitching.
Device resets during ESD or other transient testing only when an oscilloscope is used to monitor the -Reset line	• Do not ever probe the -Reset line during transient testing. -Reset is a sensitive, high-impedance line, and any connection to it during transient testing will inject a portion of the transient into the reset circuit. Instead, use network communication to Query the Neuron Chip to see if it has recorded an external reset due to a transient.
Device is watchdog resetting every second (1 OMHz clock)	• 3150 chip based device cannot reliably access external memory [5.2]. Check memory device connections & speed. • The Neuron C application may be incorrectly bypassing the scheduler. Check the application program. • If the Neuron Chip seems to intermittently watchdog, verify that all Vcc and Ground pins are actually connected on the PCB. Opens or bad solder joints on the Neuron Chip's Vcc or Ground pins can cause very intermittent operation. • If a Special Purpose Mode transceiver is being used, check the CPO receive data line. If it is stuck high, the MAC processor in the Neuron Chip will interpret this continuing RXD=1 condition as an incoming packet, Incoming packets cannot be longer than the watchdog timeout period.
Device appears to be resetting, but the -Reset line does not ever appear to go low	• When the Neuron Chip asserts a software reset, it drives the -Reset line low [4.8,3]. However, depending on the Neuron Chip version, the time that -Reset stays low can be very short (as short as 1 µs). A logic probe with a memory feature, or an oscilloscope with a good trigger circuit is generally needed to capture this software reset event. When using a Fluke ScopeMeter [3.3.3] to monitor -Reset, use the "MinMax on A" feature to enhance its ability to capture glitches.
Device does not reliably reset when -Reset is driven by an external circuit	• If another device can assert -Reset, it should use either an open-collector/drain logic buffer (HC03, HC09), or use a schottky diode to isolate the drive logic from the -Reset line. A standard silicon diode with Vd=O.6V does not leave enough voltage margin when used to drive the Neuron Chip's -Reset input (which has Vil=O.8V max.)
During a Load/Start of a device by a network manager (like LonBuilder), everything seems to go well until near the end of the loading process, when the network management software complains about the device not responding. The Load/Start fails.	• If most of the loading proceeds, but some Query Status messages from the network management software go unanswered by the device, then suspect that the reset process for the device is too long. During the Load/Start operation, the device is reset to force new configurations to take effect. The network management software often does a Query Status after the reset to check that the device is functioning correctly, and if the Neuron C program spends too much time in the when(reset) clause, the Query Status message may not generate a response before the network management software times out. This timeout period varies, but is usually 1-10 seconds.

[4.9] Clock Generation Issues

[4.9.1] Clock Circuit Waveforms

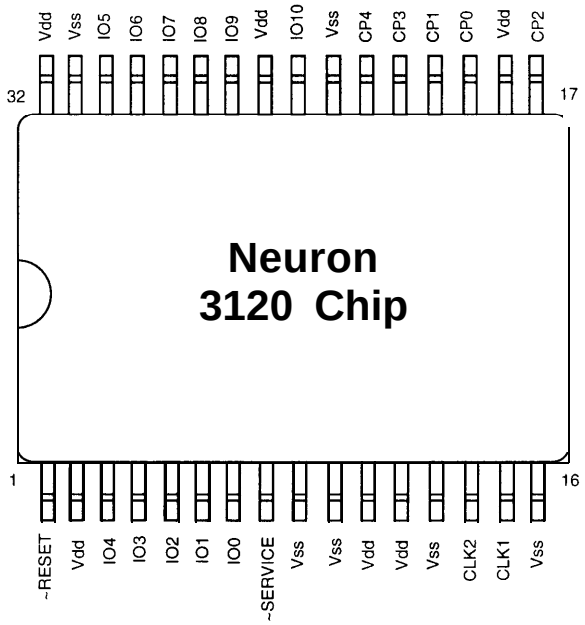
(when measured with a Z-lead oscilloscope probe)



[4.9.2] Common Clock Problems

SYMPTOM	POSSIBLE CAUSE
Clock waveform is the wrong frequency	• Crystal is the wrong frequency • Capacitors are the wrong value. NPO caps are recommended here for temperature stability. • CLK2 is overloaded with other gates (one HC input allowed) • A digital oscilloscope measuring the waveform could be aliasing. Change the time base a few steps to see if the frequency looks correct at a different time/div.
Clock signals are stuck: CLK1 = 5V, CLK2 = 5V	• Neuron Chip may be asleep. Press the Service Pin or Reset to force a wakeup. • CLK2 output may be shorted to 5V. The Neuron Chip may get hot from a short on its output line. • Neuron Chip may be broken.
Clock signals are stuck: CLK1 = OV, CLK2 = OV	• CLK2 output may be shorted to OV. The Neuron Chip may get hot from a short on its output line. • Neuron Chip may be broken.
Clock signals are stuck: CLK1I = 5V, CLK2 = OV	• CLK1 may be shorted to 5V. • Neuron Chip may be broken.
Clock signals are stuck: CLK1 = OV, CLK2 = 5V	• CLK1 may be shorted to OV. • Neuron Chip may be broken.
Clock signals are stuck: CLK1 = 2.5V, CLK2 = 2.5V	• Crystal or resistor may be open. • (Neuron Chip is probably okay; the 2.5V bias is correct)
Excessive ringing on clock lines	• Non-Z-lead scope probe will show ringing in the waveform. • Clock lines too long. If clocks are being buffered & routed around the PCB, suspect a bad termination. Note that HC gates generally do not work well for transmission lines.
Neuron Chip operation is intermittent when using a clock oscillator for CLK1, but is fine when using the crystal circuit above	• The clock oscillator must have CMOS-compatible output drive levels ("rail-to-rail"). If an oscillator with TTL output levels is used, clock operation may be very intermittent.

[5.1] Troubleshooting 3120xx Chip Devices



[5.1 .1] Comm Parameter Issues

- Neuron 3120 Chips come from the manufacturer with default comm parameters set to DC-1250 (assuming a 10MHz clock).
- In general, the Neuron 3120 Chip must have at least its comm parameters changed on a 3120 Chip Programmer before being soldered onto the PCB.

[5.1 .2] Programming The Different 3120 Chip Versions

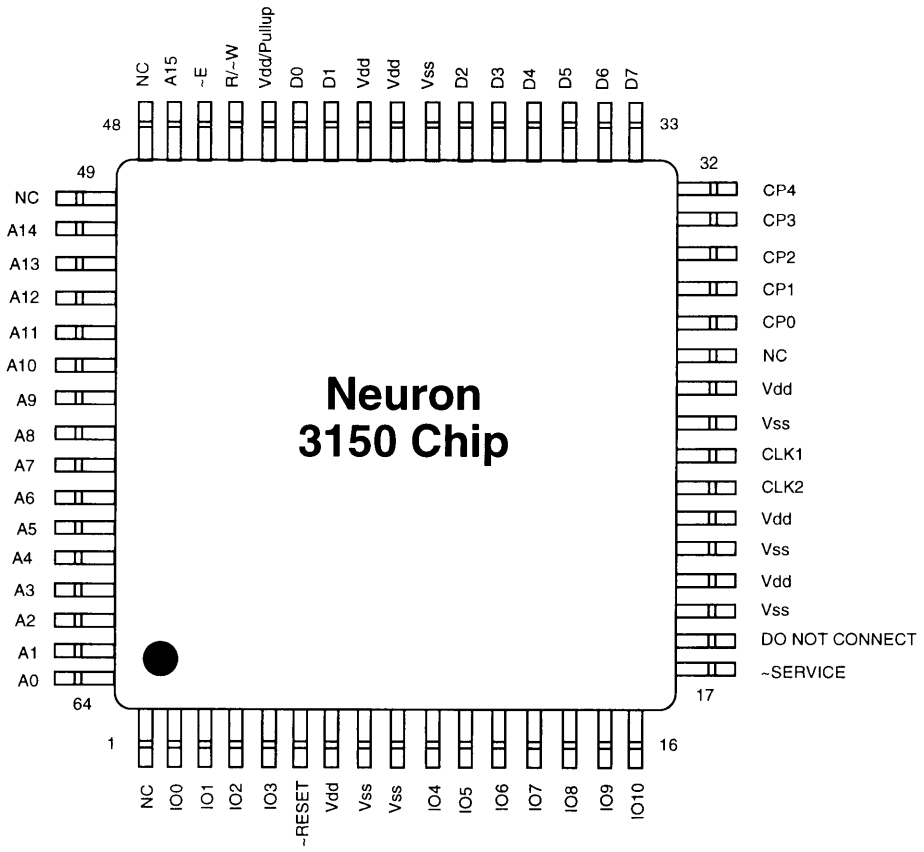
- The different 3120 Chip versions require different “Properties” settings to generate the .NEI file that is used by the 3120 Chip Programmer:

	Masked ROM Firmware Version #	To Build LB2.2 Program & .NEI File	To Βυιλδ≥ ΛΒ3.Ο Program & .NEI File
3120 Chip	Version 3	Use Properties: FW Version = 3 (3120 default in LB2.2)	Use Properties: FW Version = 3 (NOT 3120 default in LB3.0)
3120B1 Chip	Version 4	Use Properties: FW Version = 4 (get n3120_ v4.zip from the Echelon FTP Site)	Use Properties: FW Version = 4 (3120 default in LB3.0)
3120E1 Chip	Version 6	Not Accessible	Use Properties: FW Version = 6 (3120E1 default in LB3.0)
3120E2 Chip	Version 6	Not Accessible	Use Properties: FW Version = 6 (3120E2 default in LB3.0)

[5.1 .3] Common Problems With 3120 Chip Devices

SYMPTOM	POSSIBLE CAUSE
The first check-boards for a new Neuron 3120 Chip-based device do not function. The device will not run its Neuron C application, and attempts at communication with the device fail.	• Use the Troubleshooting Flowchart [2.] to guide the debugging. Check the device's power, clock, reset, etc. as shown in the flowchart.
Even after working through the Trouble-shooting Flowchart in [2.], the Neuron 3120 Chip seems to have intermittent operation.	• The connection of the 3120 Chip onto the PC board should be carefully checked. With the device powered off, check continuity between the 3120 Chip pins and the external circuitry. Carefully inspect the 3120 Chip pins for bad solder joints, and reflow any suspect joints. • After the normal troubleshooting procedure has been followed, the most likely cause of the problem is a damaged Neuron 3120 Chip. A hot-air SMT rework station should be used to remove the suspect 3120 Chip. • If replacing the 3120 Chip fixes the problem, then either the soldering of the original chip was the problem, or the 3120 Chip has been damaged somehow. It is important to wear an ESD grounding strap when working with exposed PC boards that are powered up. While an exposed circuit is on, there is a very real danger of latchup in the Neuron Chip and external circuitry. Touching or probing a powered-up circuit board without wearing an ESD strap can cause intermittent problems and chip damage.
Network communication cannot be established with a new Neuron 3120 Chip in a device	• The default communication parameters for a new 3120 Chip are DC-1250. The 3120 Chip initially can only communicate at 1.25Mbps in differential mode (assuming a 10MHz device clock). Unless the device's transceiver is DC-1250 or TP/XF-1250, the 3120 Chip needs its comm parameters changed on a programmer before being soldered onto the PCB. The comm parameters for TP/XF-1250 are different from DC-1250, so the 3120 Chip on a TP/XF-1250 device should have its communication parameters changed by a network manager on a small network before being connected to a full-size TP/XF-1250 network. It is generally best to pre-program 3120 Chips on a device programmer, even if the target network is TP/XF-1250.
During loading of a device, the incorrect comm parameters were inadvertently loaded into the Neuron 3120 Chip, and communication was lost	c There is generally no way to recover a 3120 Chip that has incorrect comm parameters. If it is a MIP device, the host processor may be able to re-set the comm parameters over the 3120 Chip's I/0 line interface to the host. Most likely, the 3120 Chip will have to be resoldered & replaced.
A device with a 3120B1chip and an FTT-10 transceiver occasionally has comm problems until the reset switch is pushed	• Even though the 3120B1 Chip has an on-board LVI, this LVI does not have pulse-stretching capability. The FIT-1O transceiver requires the use of a pulse-stretching LVI, so an external LVI is still required with the 3120B1 chip. See the FTT-10 User's Guide for more information.

[5.2] Troubleshooting 3150 Chip Devices & External Memory



[5.2.1] The External Memory Interface Engineering Bulletin[12]

- This engineering bulletin contains memory design examples with timing inequality checks for each example. Read and understand this engineering bulletin before designing or troubleshooting Neuron 3150 Chip memory circuits. The latest copy of this bulletin is available on the FTP site, or through Echelon's Technical Publication Request Center (800) 258-4566.

[5.2.2] Debug Sequence for External Memory Problems

- Simplify the configuration as much as possible. If PALs are used in the memory decode path, burn test PALs with a simplified chip select for the main PROM only. Substitute a PROM for a Flash memory at first.
- Get EEBlank running [5.2.3]. EEBlank is the simplest program that a Neuron 3150 Chip can execute. Even if the external memory circuit contains extra RAM, Flash, memory-mapped 1/0, etc., first get EEBlank running on the core memory device.
- Once EEBlank executes correctly, start using a standard Neuron Chip firmware image, and add in the rest of the memory circuit incrementally. As more of the external memory circuit is added in, watch for chip select conflicts and memory bus contention.

[5.2] Troubleshooting 3150 Chip Devices (cont.)

[5.2.3] Using the EEBlank Program with a Neuron 3150 Chip Device

- When a Neuron 3150 Chip device experiences a failure that corrupts EEPROM in a way that prevents communication with the device, it is generally necessary to blank the on-chip EEPROM. This is done with the program EEBlank. There are two versions of EEBlank that are commonly used:
  - **EEBlank from LonBuilder 2.2**: The EEBlank.NRI file (date stamped 04-09-93, 2:20am) is used to make an EEBlank PROM. When a 3150 Chip device is powered up with this PROM, the Service LED flashes ON briefly, then stays OFF for about 13 seconds for a 10MHz device. The OFF period is about 26 seconds for a 5MHz device. At the end of this period, the LED comes ON solid, indicating that the device has successfully completed blanking its on-chip EEPROM.
  - **EEBlank from LonBuilder 3.0**: The EEBlank.NRI file (date stamped 01-06-95, 3:00 am) is used to make an EEBlank PROM. When a 3150 Chip device is powered up with this PROM, the Service LED flashes ON briefly, then begins rapid flashing (at about a 4Hz rate for a 10MHz device) for a few seconds. This flashing period can range from 3-6 seconds for a 10MHz device, depending on how much of EEPROM is already blank. The LED goes ON when the EEPROM has been successfully blanked.
- **Trick:** If no EEBlank PROM is available, but you have a different PROM from another device, you can use the second PROM to force the failed device to perform a reboot. Since the second PROM contains a different program from the failed device's PROM, it will contain a different "boot ID." When the failed device powers up with the second PROM, it will recognize that the boot ID is different, and will reboot the program and configuration information out of the second PROM into onboard EEPROM. If the failed device now seems to function correctly (based on the code that is in the second PROM), then the reboot function was sufficient to clear the failure. To restore the device to its original state, swap the original PROM back in, and power the device up. Once again, the device will recognize that the boot ID in the PROM does not match the expected value, so it will re-boot its program and configuration information from the original PROM into onboard EEPROM.
- **Trick:** If the device appears to have an EEPROM problem, but it is still able to communicate over the network, it may be possible to force the device to perform a reboot operation from a network management node or other network interface node. The 2-byte "boot ID" is stored at location 0xF1FE in the Neuron 3150 Chip's EEPROM. Use a write memory operation from the remote node to write 0x0000 into these two bytes, and then power cycle the failed device. When the device checks its EEPROM boot ID against the ID in its PROM, the mismatch should force the device to reboot. (The shareware program Nodeutil [3.2.3] also has a Reboot Node command available.)

[5.2] Troubleshooting 3150 Chip Devices (cont.)

[5.2.4] Use of a Logic Analyzer to Check Neuron 3150 Chip Execution

- When external memory mis-connections or conflicts are suspected, a logic analyzer can be used to check that the basic operation of the memory bus is correct. As a practical matter, only the first few bytes of execution need to be checked for debugging basic external memory problems.
- Check the basic operation of EEBlank first (shown below). Check that the bytes are being read from the PROM correctly starting at address 0001 (address 0000 contains the version number, and is not accessed). Since the Neuron Chip contains three processors [4.7.1], each PROM byte may be accessed multiple times.
- The logic analyzer State Listing and Timing Trace below were obtained with an HP16500A Logic Analyzer with the following configuration:

  Pod1: AO-A15, CLK=~E=~OE used for J^ in State Listing mode

  Pod2: DO-D7, ~E=O~E

Partial EEBlank PROM Listing

(PROM from EEBlank.NRI file dated 01-06-95, 3:00a)

EEBlank Version 3

Execution starts with E1, E8, 02....

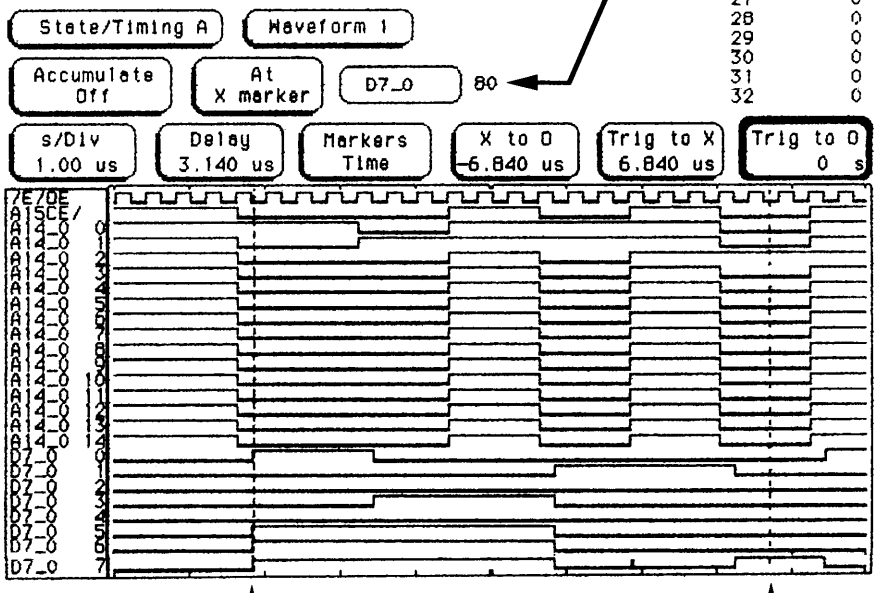
```
000000  03 E1 E8 02 80 B4 10 E2-B4 09 E3 A0 59 03 76 00
000010  0C B4 2E E2 B4 18 E3 80-F7 FF B5 71 FA 76 01 0F
000020  E1 E8 9F B4 4B E2 B4 1D-E3 80 F7 FF B6 71 FA E4
000030  E1 E9 1D B4 FF E2 B4 18-E3 81 F7 E8 F5 80 D7 80
000040  D6 B5 F0 08 F3 82 E7 B4-FC E7 96 5B 32 65 9B 00
000050  73 1A 23 96 3E D6 80 02-FE 97 64 84 F7 FF A4 97
000060  3E D7 97 5B 04 66 80 D7-86 F7 FF A4 37 00 90 70
000070  D9 70 D4 80 B5 F0 08 F3-82 E7 B4 FC E7 9B 00 52
```

Logic Analyzer State Listing

Label> / Base>	/E/OE Binary	A15CE/ Binary	A14_0 Hex	D7_0 Hex
1	0	0	0001	E1
2	0	0	0001	E1
3	0	0	0001	E1
4	0	0	0002	E8
5	0	0	0002	E8
6	0	0	0002	E8
7	0	1	7FFF	E8
8	0	1	7FFF	E8
9	0	1	7FFF	E8
10	0	0	0003	02
11	0	0	0003	02
12	0	0	0003	02
13	0	1	7FFF	02
14	0	1	7FFF	02
15	0	1	7FFF	02
16	0	0	0004	80
17	0	0	0004	80
18	0	0	0004	80
19	0	1	7FFF	01
20	0	1	7FFF	01
21	0	1	7FFF	01
22	0	1	6803	00
23	0	1	6803	00
24	0	1	6803	00
25	0	1	7FFF	00
26	0	1	7FFF	00
27	0	1	7FFF	00
28	0	0	0005	B4
29	0	0	0005	B4
30	0	0	0005	B4
31	0	1	7FFF	02
32	0	1	7FFF	02

Example: Data is 80h right before the 18th access

Logic Analyzer Timing Trace



Trigger on ~OE = ~CE = 0

Data is 80h right before the 18th access

[5.2.4] Use of a Logic Analyzer to Check Neuron 3150 Chip Execution (cont.)

- After EEBlank is running correctly [5.2.3], a PROM containing the standard Neuron Chip Firmware ("System Image") can be checked. The logic analyzer State Listing and Timing Trace shown below are for a 16KB System Image PROM running on an FTT-10 Control Module. The PROM was built for a Neuron 3150 Chip using LonBuilder 3.0 and Version 6 firmware.
- Once the System Image appears to be working correctly, the logic analyzer can be used to check the operation of any other external memory on the device.
- Note that a Bug Katcher™ socket adapter from Emulation Technology was used to allow the logic analyzer to monitor these PROM signals. For the 32-pin PLCC PROM socket on Echelon's FTT-10 Control Module, use Bug Katcher part number BC4-32-PCC7-OOO0. Emulation Technology can be reached at (408) 982-0660.

Partial System Image PROM Listing

(From a 16KB System Image PROM for an FTT-10 Control Module)

PROM Image Built with Version 6 firmware

Execution starts with 75,31,BA (jump to 31BAh)

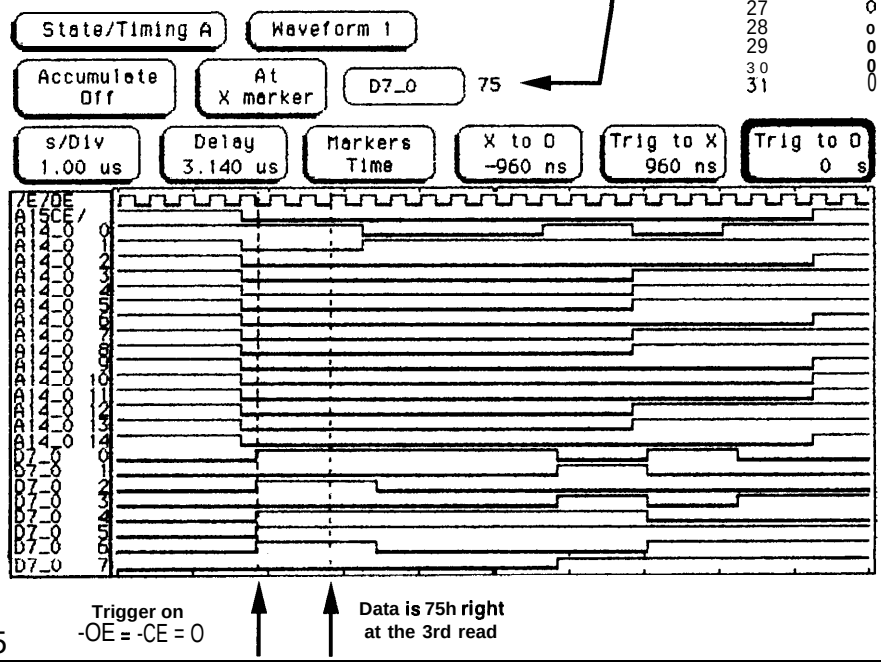
```
000000  06 75 31 BA 80 21 85 75-F0 26 58 EE A3 50 A6 3E
000010  A6 7F 58 EE A3 50 E6 3F-E6 7F 58 EE A3 50 A6 7F
000020  58 EE A3 50 E6 7F E7 80-70 FD 31 F6 F6 A3 55 E3
000030  7F F6 F6 3F 00 39 F5 F6-F6 E7 F0 A7 00 2D B0 31
000040  A3 50 58 1D B4 E9 B6 23-50 21 3E 32 0F B6 3E 2B
000050  80 A5 59 80 46 24 3F 32-03 B6 3F B6 31 F0 98 00
000060  98 01 31 80 80 B7 E9 2C-41 7E A0 59 03 4F 00 89
000070  B7 E8 8B 3E 65 E4 E4 B5-00 00 77 2C 2C 80 F7 FF
```

Example: Data is 75h right at the 3rd read

Logic Analyzer State Listing

Label> / Base>	/E/OE Binary	A15CE/ Binary	A14_0 Hex	D7_0 Hex
0	0	0	0001	75
1	0	0	0001	75
2	0	0	0001	75
3	0	0	0001	75
4	0	0	0002	31
5	0	0	0002	31
6	0	0	0002	31
7	0	0	0002	31
8	0	0	0002	31
9	0	0	0002	31
10	0	0	0003	BA
11	0	0	0003	BA
12	0	0	0003	BA
13	0	0	31BA	E1
14	0	0	31BA	E1
15	0	0	31BA	E1
16	0	0	31BB	E8
17	0	0	31BB	E8
18	0	0	31BB	E8
19	0	1	7FFF	E8
20	0	1	7FFF	E8
21	0	1	7FFF	E8
22	0	0	31BC	02
23	0	0	31BC	02
24	0	0	31BC	02
25	0	1	7FFF	02
26	0	1	7FFF	02
27	0	1	7FFF	02
28	0	0	3160	54
29	0	0	31BD	B4
30	0	0	31BD	B4
31	0	1	7FFF	01

Logic Analyzer Timing Trace



Trigger on -OE = -CE = 0

Data is 75h right at the 3rd read

[5.2.5] Common Problems with External Memory &31 50 Chip Devices

SYMPTOM	POSSIBLE CAUSE
The first check-boards for a new Neuron 3150 Chip-based device do not function. The device will not run its Neuron C application, and attempts at communication with the device fail.	• Use the Troubleshooting Flowchart [2.] to guide the debugging. Check the device's power, clock, reset, etc. as shown in the flowchart. As the problems are isolated to the external memory circuit, follow the procedure outlined in section [5.2.2].
Even after working through the Trouble-shooting Flowchart in [2.] and the procedure described in [5.2.2], the Neuron 3150 Chip seems to have intermittent operation.	• The connection of the 3150 Chip onto the PC board should be carefully checked. With the device powered off, check continuity between the 3150 Chip pins and the external circuitry. Carefully inspect the 3150 Chip pins for bad solder joints, and reflow any suspect joints. • After the normal troubleshooting procedure has been followed, the most likely cause of the problem is a damaged Neuron 3150 Chip. A hot-air SMT rework station should be used to remove the suspect 3150 Chip. • If replacing the 3150 Chip fixes the problem, then either the soldering of the original chip was the problem, or the 3150 Chip had been damaged somehow. It is important to wear an ESD grounding strap when working with exposed PC boards that are powered up, While an exposed circuit is on, there is a very real danger of latchup in the Neuron Chip and external circuitry. Touching or probing a powered-up circuit board without wearing an ESD strap can cause intermittent problems and chip damage.
The device seems to be running normally, but the Service LED is ON solid.	• The device most likely has logged a self-test failure after its most recent reset. The Built-In Self-Test (BIST) procedure in the Neuron 3150 Chip performs a RAM test as part of the initialization & BIST routines [4.8.3], and if there is any problem with writing & reading back any RAM that is listed in the device's memory map, the self-test will fail. Try using the #pragma ram_test_off temporarily in the Neuron C application code to see if the BIST failure goes away, If it does, debug the RAM access problem. (A common error is to use a PAL to generate the WE signal for external RAM. The logic delay in a PAL is generally too long to meet WE timing constraints.)
A Flash-based Neuron 3150 Chip device works correctly when a PROM is used in the Flash socket. The device does not work when a Flash memory part is used for the main external memory.	• Check that the speed of the Flash memory part is correct for the device's clock rate (see the External Memory Interface engineering bulletin). • Check that the Software Data Protection (SDP) feature is enabled at the PROM programmer used to program the Flash memory part. If the firmware image that is being loaded into the part is ≥ 86 pages (21 .5KB), the firmware will expect the part to have been programmed with the SDP feature enabled. • Check the Flash memory part's pinout to be sure that the PC board was designed using the correct pinout. The 29C256 and 29C257 Flash parts are the same size, but they have different pinouts.
The device's application seems to be working correctly, but the device is sending a continuous stream of Service Pin packets onto the network.	• Check for a short between pin 17 (-Service) and pin 18 (Do Not Connect) of the 3150 Chip. Pin 18 is an output which toggles with Neuron Chip operation, so a short from this pin to the Service pin causes continuous Service Pin packets to be transmitted.

[5.3] Troubleshooting Devices That Use Echelon's Twisted Pair Control Modules

[5.3.1] LVI Issues With Control Modules

- As discussed in section [4.8.1], an LVI function is required on all Neuron Chip-based devices. The LVI function belongs with the power supply function in a device, so most of Echelon's control modules do NOT include an on-board LVI.

- For most of Echelon's control modules, an LVI is expected on the motherboard that the control module plugs into. See the Control Module User's Guide[7] for more information on LVIs and Reset circuit capacitive loading.

[5.3.2] Common Problems with Control Modules

SYMPTOM	POSSIBLE CAUSE
A device that uses an Echelon control module does not run its application, and will not communicate over the network.	• Use the Troubleshooting Flowchart [2.] to guide the debugging, but since the core Neuron Chip circuit on the control module is probably good, focus on the external inputs to the control module, such as power and Reset. • Ensure that the motherboard the control module plugs into has an LVI. If there is no LVI on the motherboard, then the EEPROM of the control module's Neuron 3150 Chip may have been corrupted. Use EEBlank [5.2.3] to re-initialize the 3150 Chip's EEPROM and add an LVI. • If EEBlank will not run in the control module, suspect an error in programming the PROMS, Ensure that the correct PROM parts are being used, and that the PROM programmer is working correctly. • If replacing the control module fixes the problem, then the original control module was probably damaged. Always wear an ESD grounding strap when working with control modules that are exposed and powered-up, since all of the Neuron Chip's unprotected circuitry is exposed.
A TP/XF-78 or TP/XF-1250 control module with an old date code runs the application correctly, but will not communicate over the network.	• Until about 1995, the TP/XF-78 and -1250 control modules expected the transceiver center taps to be shorted on the motherboard at the connector that mates with the module's P2 connector. Pins 1 and 2 in the motherboard's P2 mating connector should be shorted together to ensure that the transceiver's transformer operates correctly. More recent TP/XF-78 and -1250 control modules have the center tap shorted on the control module.
A device based on a control module seems sensitive to ESD hits.	• Control modules are very robust against ESD, as long as the "P2 standoff" is connected to the motherboard's chassis ground. See the Control Module User's Guide for info.
A device containing a conformably-coated control module is failing.	• Control modules have sockets and connectors that are not meant to be conformably coated, and coating the modules usually voids their warranty. Contact Echelon Technical Support.

[5.4] PC Board Layout Issues

[5.4.1] Common PC Board Layout Problems

- In addition to the PC board layout guidelines contained in the appropriate User's Guides, the following paper can be very helpful: "Designing LONWORKS Devices To Comply With The EMC Directive." This paper was presented at the Fall 1995 LONUSERS International conference in Frankfurt, Germany. PC board layout and testing issues are covered in detail, and techniques to improve device robustness against ESD and other transients are presented. Contact Echelon Technical Support for a copy of this paper.

- Echelon Technical Support also offers a design review service under its LonSupport™ program. The design review covers issues related to the "Echelon Content" of the design, especially issues related to the PC board layout of the transceiver, and the package grounding. Contact Echelon Technical Support for information on this service.

- Beyond basic electrical connection issues, PC board layout problems usually manifest themselves as a sensitivity to ESD or other transients. These transients can cause logic errors, or even latchup of the Neuron Chip. Layout problems can also be a source of radiated EMI problems.

SYMPTOM	POSSIBLE CAUSE
The device has a sensitivity to ESD hits to the network connector, power connector or package.	. The layout of the transceiver, power supply and chassis ground connection should follow the rules of a star ground system. See the LONUSERS paper mentioned above for an illustration of star grounding. If a star ground configuration cannot be used for some reason, the paper also describes a cut-ground or "quiet-ground" technique that can be used. The Neuron Chip's Vss pins must all be tied together using a low-impedance ground connection (preferably a small plane of ground underneath the SMT Neuron Chip), and decoupling caps should be placed around the Neuron Chip.
The device has a sensitivity to ESD hits to a keypad or LEDs.	• Any circuit that can receive an ESD hit (like an I/0 line driving an LED) must be protected with diode clamps or using other techniques. Any entry or exit point for transients in a device must guide the transient current to the center of the star ground without allowing the current to flow through circuitry like the Neuron Chip. See the LONUSERS paper or the transceiver User's Guides for more information.
The device does not have an ESD problem, but EMI testing shows some radiated frequencies over the FCC or EN 55022 limits.	• Star grounding also helps keep down radiated EMI. If the device does not have an ESD problem, then it probably has a good star ground design. Designing a PC board and package to minimize EMI additionally involves guarding of clock traces and any memory bus traces in the device. See the LONUSERS paper and transceiver User's Guides for additional information.
A Neuron 3150 Chip device sometimes experiences external memory access errors, including bad writes to external RAM or Flash memory.	• Reliable memory bus operation requires a good ground layout on the PCB. The Neuron Chip must have a low-impedance ground connecting its multiple Vss pins, and this wide ground connection should extend to the ground pins of the external memory devices. Vcc/Vdd decoupling caps should be placed at each device Vcc pin. '

[5.4] PC Board Layout Issues (cont.)

[5.4.2] The "Top Hat Rework" Technique for Layout Debugging

- **Extremely Effective Technique for EMI & ESD Debugging (especially for PC boards where grouding and decoupling are suspected causes of Neuron Chip errors or latchups)**

- **Rework Simulates Very Good Grounding & Decoupling on The PCB**

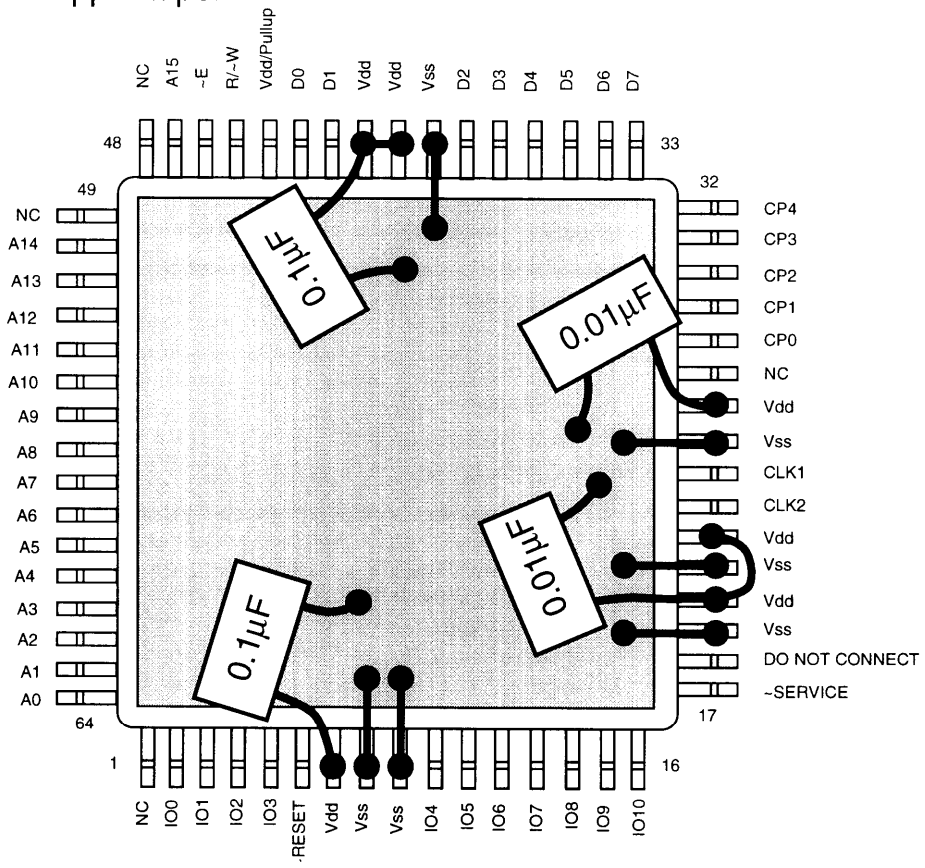
- **Rework Steps (Neuron 3150 Chip Shown):**

1) Cut a square of copper tape to cover the top of the Neuron Chip. This "Top Hat" forms an accessible ground plane on top of the chip.

2) Using thin wire (i.e. bare wire-wrap wire), connect each Vss pin to the top hat ground plane. Keep the wire connections as short as possible.

3) Connect four 0.1µF (or 0.01µpF)ceramic radial caps as shown between the Vdd pins and the top hat ground plane. Keep all leads short.

4) If the PCB grounding to external memory devices is not low impedance, perform the same kind of top hat rework on the memory devices, and connect the top hat ground planes with a **0.5"** wide strip of copper tape.



NEURON 3150 CHIP

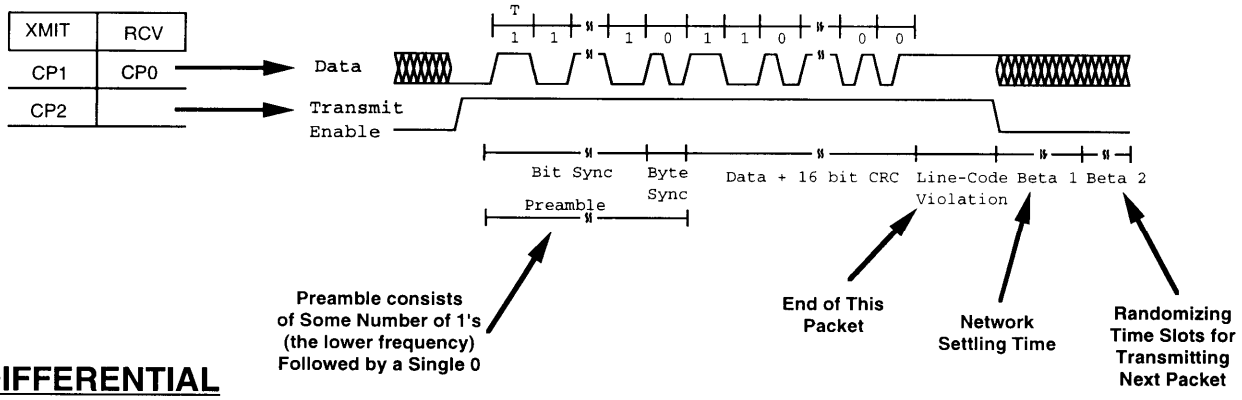
[6.] Troubleshooting Twisted Pair Networks & Transceivers

[6.1] General TP Network Concepts

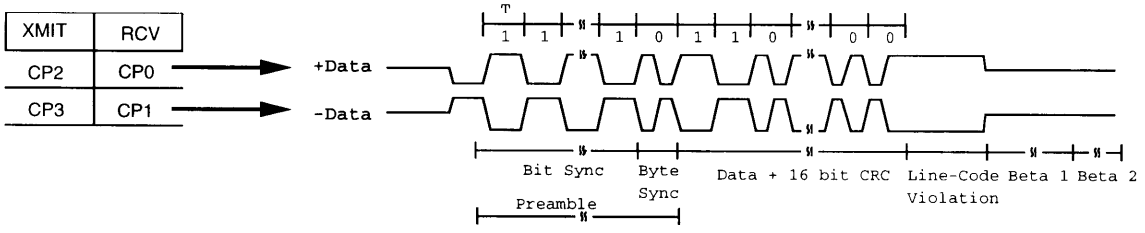
[6.1 .1] Differential Manchester Encoding

- Echelon's twisted pair transceivers interface to the Neuron Chip through either the Single-Ended mode or the Differential mode of the Neuron Chip's Communication Port. In both of these modes, differential Manchester coding of the data is used. In differential Manchester coding, the presence or absence of a "data" transition in the center of each bit period signifies a O or 1 bit, respectively. Thus, the body of a 78kbps transmission packet consists of a mix of 39kHz (1) and 78kHz (0) components. The "Line Code Violation" is an extra-long bit that signals the end of the packet data.

SINGLE-ENDED



DIFFERENTIAL



- The receiver on the Neuron Chip will correctly identify an incoming O or 1 bit if the transition on its receive data line(s) falls within a window around the next expected transition time. See the Neuron Chip databook for more information about these "jitter windows. "

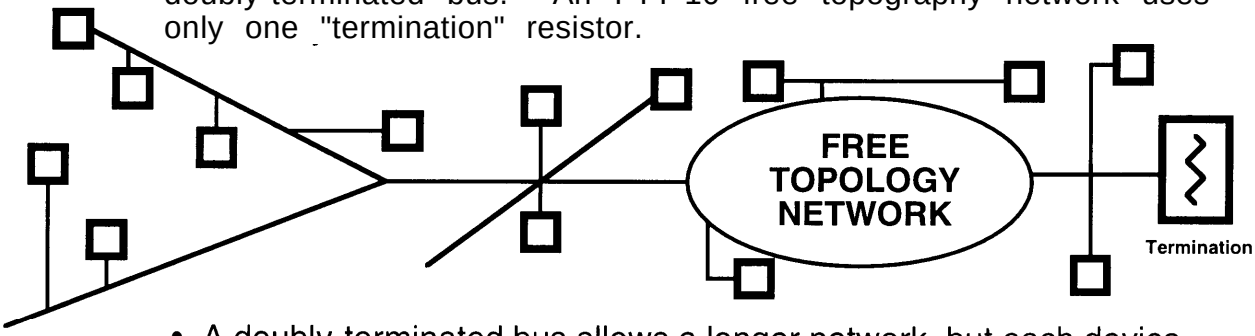
- The FTT-1O and LPT-1O transceivers communicate with Neuron Chips using the Single Ended communication mode. Free topology networks [5.1 .2] can have extra distortion in the received waveform (due to signal reflections in the free topology wiring), but the FTT-1O and LPT-1O transceivers perform extra signal processing to clean up the packet waveform that the Neuron Chip receives on its CPO line.

- The TP/XF-78 and TP/XF-1250 transceivers interface with Neuron Chips using the Differential communication mode. The Neuron Chip's on-board analog receiver circuit processes the incoming waveform. The Neuron Chip receiver circuit alone does not have sufficient processing to receive a packet from a free topology network.

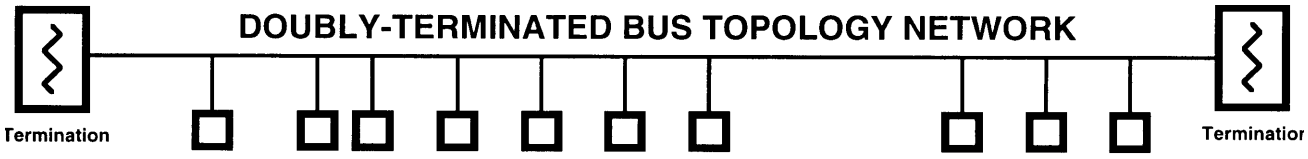
[6.1] General TP Network Concepts (cont.)

[6.1 .2] Free Topology & Doubly-Terminated Bus Topology

- A twisted pair network can be wired either as a doubly-terminated bus or as a free topology. Each configuration has advantages & drawbacks:
- A free topography network is generally easier to wire, but the maximum node-to-node length of the network is not as long as with a doubly-terminated bus. An FTT-10 free topography network uses only one "termination" resistor.



- A doubly-terminated bus allows a longer network, but each device connected to the network must be placed close to the main network wire. A "stub" is used to connect the device to the doubly-terminated bus wire. Stub lengths range from 3m for FTT-10 networks down to 0.3m for TP/XF-1250 networks.



[6.1 .3] Network Wire & Terminations

- See the engineering bulletin on Wiring Guideline[13] for a summary of wire information & suppliers for Echelon's twisted pair networks.
- See the appropriate User's Guide[3,4,6] for additional information about network wire and terminations for FTT-1O, TP/XF-78 and TP/XF-1250 networks.
- It is very important that the termination circuits shown in the User's Guides be used!
  - In a doubly-terminated bus network, the terminations minimize reflections from the ends of the network transmission line. If a termination is missing or damaged, reflections from the ends of the transmission line will cause waveform distortion that is different at different locations along the network (i.e., some pairs of nodes may no longer be able to communicate).
  - In an FTT-1O free-topology network, the single "termination" is used to convert the current-output drive of the FTT-1O into the network voltage waveform. If the termination is missing or damaged, the network waveform will be distorted, which will degrade communication.

[6.1] General TP Network Concepts (cont.)

[6.1.4] Noise On Real-World Networks

- When a network is installed in a real-world environment (as opposed to the development lab environment), it is exposed to several noise sources that can make measurement of analog network waveforms more difficult. The measurement techniques shown in [3.3.2-3.3.3] are necessary to ensure that common-mode network noise does not interfere with the measurement of the differential analog network communication waveform.

  - **Power Line Noise & Ground Shifts:** The "Safety" or "Earth" ground reference will vary between different parts of a building. This difference in voltage can have a DC component, but more often the voltage varies at the power line rate (50Hz or 60Hz), with an amplitude that can reach many 10's of volts, or higher. DC shifts and power line frequency noise are naturally rejected by the transformer-coupled transceivers in FTT-1O and TP/XF devices. Link Power LPT-1O devices are required to be "floating" with respect to their local Earth ground reference.

  - **High Frequency Burst Noise:** When the network cable is run near DC motors or other sources of burst noise, common mode voltage noise can be coupled into the twisted pair. Even though this burst noise has frequency components within the communication band of the network, the common-mode rejection of the coupling transformers used in the FTT-1O and TP/XF transceivers is usually sufficient to prevent significant impairment of communication.

[6.1.5] Common Network Wiring Problems

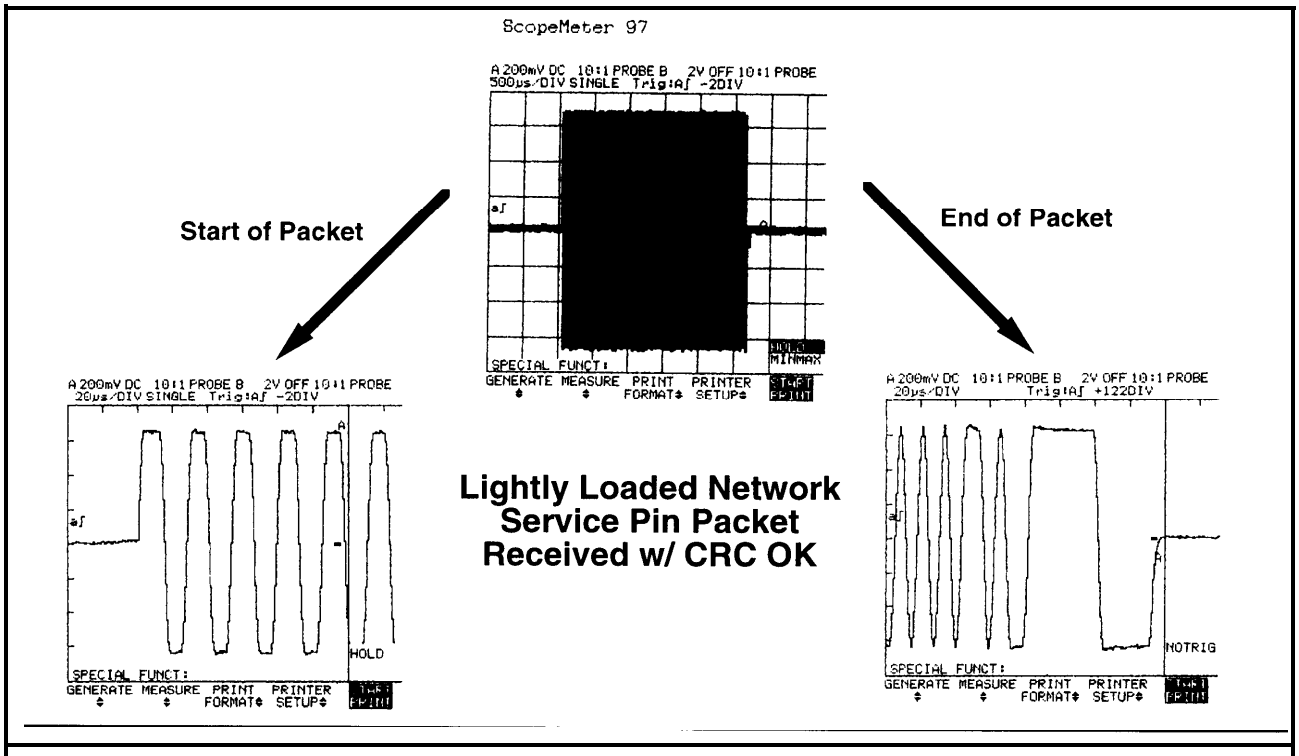
SYMPTOM	POSSIBLE CAUSE
Devices work fine on a small network, but communication fails on a large network installation.	• Use the right-hand side of the Troubleshooting Flowchart shown in [2.] to help in debugging network communication problems. As long as the rules for wire type, length, termination, etc. given in the transceiver User's Guides are followed, a large network should have the same reliable communication as a small network, • When communication on a large network is a problem, suspect bad connections, bad terminations, extra capacitive loading of some kind (like transient protection devices not listed in the User's Guides), or noise sources coupling into the network. Also suspect bugs in the Neuron C application code of the device, and be sure to check that the network addressing and configuration of of the devices is correct.
The network wire, terminations, etc. all seem to be within Echelon's design rules, and the network management software seems to be configuring the devices correctly, but some device communications are still unreliable.	• If a few devices have communication problems no matter where they are moved on the network, suspect a bad network connector or a bad device. If devices only have problems when moved to certain spots in the network, suspect transmission line problems (like a broken termination), or point noise sources near the failure spots. • If a hardware reason for the failures is not apparent, use a Protocol Analyzer [3.1] to watch network traffic for addressing anomolies that might indicate network management problems.

[6.2] Troubleshooting FTT Networks

[6.2.1] FTT-1O Network Topologies & Terminations

- FTT-1O networks can be Free Topology or Doubly-Terminated Bus Topology.
- . See the FTT User's Guide[3] for detailed information on topology & wire limits

[6.2.2] Typical FTT-1O Analog Network Waveforms



[6.2] Troubleshooting FTT Networks (cont.)

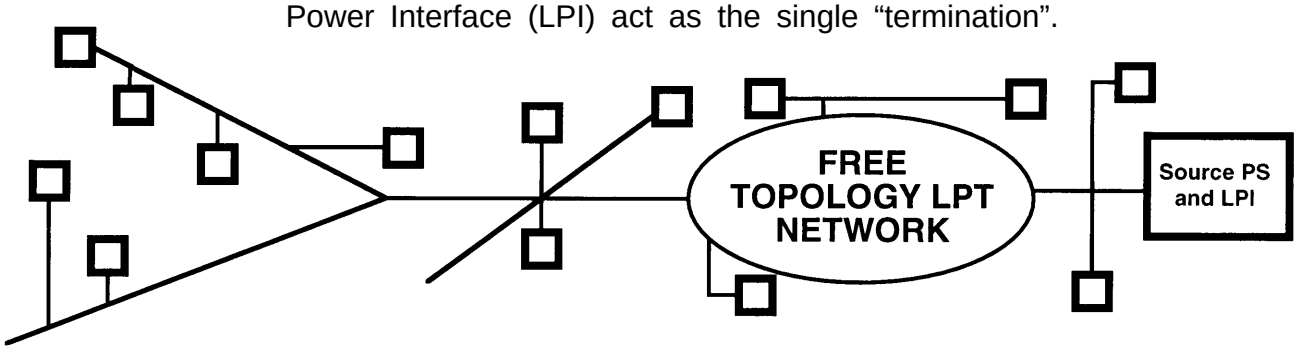
[6.2.3] Common Problems with FTT Networks

SYMPTOM	POSSIBLE CAUSE
A device cannot communicate on an FTT network.	• Use the right-hand side of the Troubleshooting Flowchart shown in [2.] to help in debugging this device's comm problem. First double-check that the wire, connections and termination are correct. Then use Service Pin presses to generate transmit packets, so that the CP line waveforms can be checked [6.1.1]. Another device on the network can be used to generate incoming traffic to the device under test in order to check the CP line waveforms in receive mode. Finally, the analog waveforms on the network can be checked for clues about the lost communication.
The device can transmit, but not receive (for example, LonBuilder tool Install succeeds, but nothing else works; see [4.5])	• Suspect an incorrect clock configuration for an FTT-1O: - Check CSO and TXD/CS1 connections for FTT-1O. - Reset the device by manually grounding the reset line. If the device recovers, suspect an incorrect reset circuit or transient protection circuit implementation. See the FTT-1O User's Guide for correct circuit implementation. • An incorrect clock configuration on the FTT-1O's CSO & CS1 pins usually will result in the FTT-10 transmitting a very distorted waveform, even into a small, lightly-loaded network. An FTT-1O with an incorrect clock configuration will not receive packets from the network.
The device communicates fine on short networks, but does not communicate on a "full-size" network installation	• Check that the total wire length & wire type agree with the specifications in the FTT User's Guide. Suspect an over-loaded network, or incorrect wire substitution. . Check the termination(s). Incorrect or broken terminations will make communication integrity dependent upon a device's position on the network. . Check the devices to be sure that no extra capacitance is being connected to the network other than the standard FTT circuit, and a maximum of a 3 meter stub (in doubly-terminated bus topology). A common error is to add high-capacitance transient protection devices (like zeners) across the network connection.
When attempting to transmit a packet, the device's CP lines do not behave correctly.	" The FTT-10 uses Single Ended mode for the CP lines [6.1 .1]. CPO, CP1 and CP2 are RXD, TXD and TXEN, respectively. If the device is incorrectly configured for Differential mode or Special Purpose mode, the CP lines will not function correctly for controlling the FTT-1O.
An FTT-1O device that uses a DC-DC converter power supply has a high CRC error rate, and has trouble receiving packets on heavily loaded networks.	• Suspect that DC-DC switching noise is interfering with the 78kbps communication band of the FTT-1O. Check the switching frequency of the DC-DC; if it is 1 MHz, then it is not likely the source of the problem. If it is 50-1OOkHz, then interference with communication is possible. The FTT-1O has good power supply rejection in the communication band, so the most likely noise coupling mechanism is magnetic. Check that the DC-DC switching inductor is not adjacent to the FTT-1O transceiver and its transformer. The transformer used on the FTT-1O rejects magnetic noise coupling well, so the DC-DC inductor would need to be fairly close to cause a problem. Try re-orienting or moving the DC-DC inductor to see if the comm problem goes away.

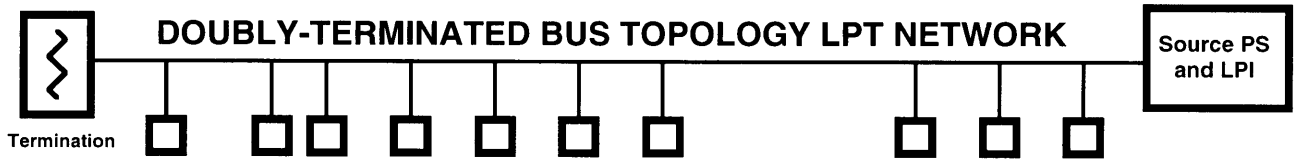
[6.3] Troubleshooting LPT Networks[4,5]

[6.3.1] Link Power Topologies

- Link Power networks can be wired in free topology, or in doubly-terminated bus topologies:
  - In a free topology network, the Source Power Supply and its Link Power Interface (LPI) act as the single "termination".



- In a doubly-terminated bus topology network, the Source Power Supply and its Link Power Interface (LPI) act as one "termination, " while a single free topology termination is used at the other end of the bus. See the LPI-I O User's Guide[5] for LPI jumper settings when used in a doubly-terminated bus configuration.



[6.3.2] Source Power Issues

- The Source Power Supply must meet certain criteria for startup behavior, output noise, current limiting, etc. These criteria are listed in LPI-10 User's Guide. If an LPI-10 Link Power Interface module from Echelon is used between the Source Power Supply and the network, then some of the current limiting and voltage regulation tasks become easier for the Source Power Supply. If the inductor-based, passive LPI circuit shown in the Appendix of the LPI-IO User's Guide is used, then more of the voltage regulation issues need to be addressed by the Source Power supply.

[6.3.3] Wiring Issues

- Wiring issues for Link Power networks are similar to those for FTT-1O networks, with the addition of power transmission considerations. See the LPT-1O User's Guide for a complete discussion of wiring and distance issues.

[6.3] Troubleshooting LPT Networks (cont.)

[6.3.4] LPT-1O **Power Conversion Issues**

- **See** chapters 2 & 4 of the LPT-1O User's Guide for a complete discussion of power conversion issues. There are several highlights from these chapters that turn up most often in troubleshooting LPT-1O devices:
  - The PCB layout of the DC-DC portion of the LPT-1O device is important. The loop area of the main switching inductor and capacitors (L1, Cl, C2 in the User's Guide) must be kept small in order to avoid ringing and Vcc noise problems. If PCB layout problems are suspected, compare the device layout to the recommended layout in chapter 2 of the LPT-1O User's Guide.
  - The choice of the main switching inductor and capacitors (L1, C1, C2) must follow the guidelines listed in chapter 2 of the User's Guide. The DCR of the inductor L1 and the ESR of the output capacitor C2 are especially important to ensure good performance of the LPT-1O's DC-DC converter. Note that no more than 1.OµF of extra decoupling capacitance is allowed over the C2=22µF capacitance.

[6.3.5] **Typical LPT-1O Analog Network Waveforms**

- **See** the typical FTT-1O Analog Network Waveforms [6.2.2]. LPT-1O waveforms are basically the same, with an additional DC voltage between the network wires.

[6.3.6] **Common Problems with LPT-1O Networks**

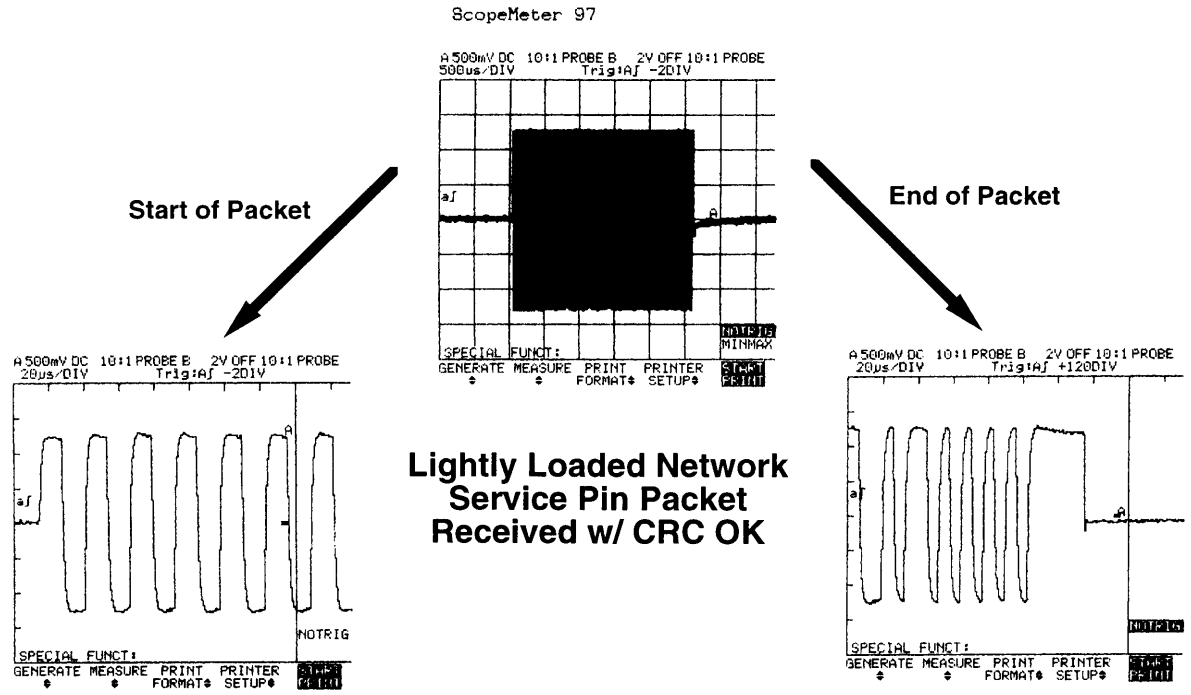
SYMPTOM	POSSIBLE CAUSE
A Link Power network powers up, but an LPT-1O device connected to the network does not communicate reliably.	• Use the right-hand side of the Troubleshooting Flowchart shown in [2.] to help in debugging this device's comm problem. First double-check that the wire, connections and LPI are correct. Then use Service Pin presses to generate transmit packets, so that the CP line waveforms can be checked [6.1.1]. Another device on the network can be used to generate incoming traffic to the device under test in order to check the CP line waveforms in receive mode. Finally, the analog waveforms on the network can be checked for clues about the lost communication. • Note that LPT-1O devices must "float" with respect to local "Earth" ground, since they are DC-connected to the Link Power Supply through the LPI and network wiring. This means that a differential probe or a battery-powered oscilloscope [3.3.2,3.3.3] must be used for probing the CP line waveforms on an LPT-1O based device. • Refer to the troubleshooting information for FTT-1O networks [6.2.3], since the FTT-10 and LPT-10 have very similar transceiver characteristics.
Devices can be added to a Link Power network while it is powered up, but the network does not power up when power cycled	• "Hot Plugging" of LPT-10 devices is not encouraged. It is possible to overload a Link Power network while the power is on, and the network may continue to run. However, the power-up of a network is the most difficult time for the Source Power Supply and LPI, and the overloaded network will likely prevent startup. Refer to the LPT-1O User's Guide for maximum loading information.

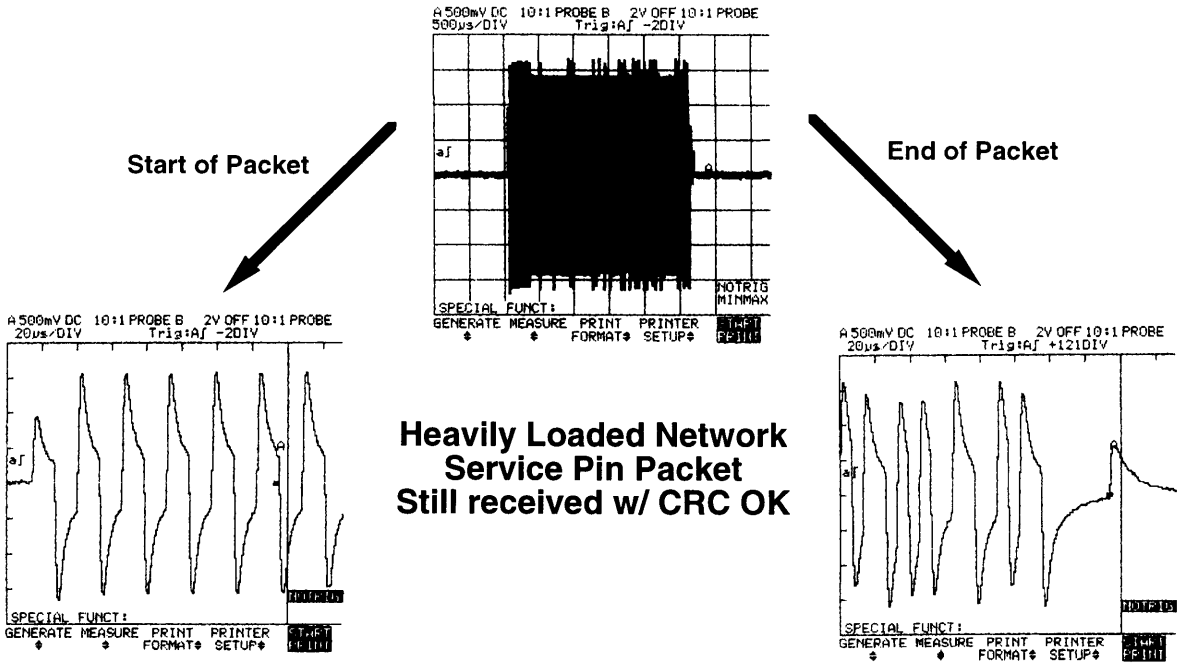
[6.4] Troubleshooting TP/XF-78 Networks

[6.4.1] Doubly-Terminated Bus Issues

- TP/XF-78 networks must be wired **in Doubly-Terminated Bus topology.**
- See the TPT User's Guide[6] for detailed information.

[6.4.2] Typical TP/XF-78 Analog Network Waveforms





[6.4.3] Common Problems with TP/XF-78 Networks

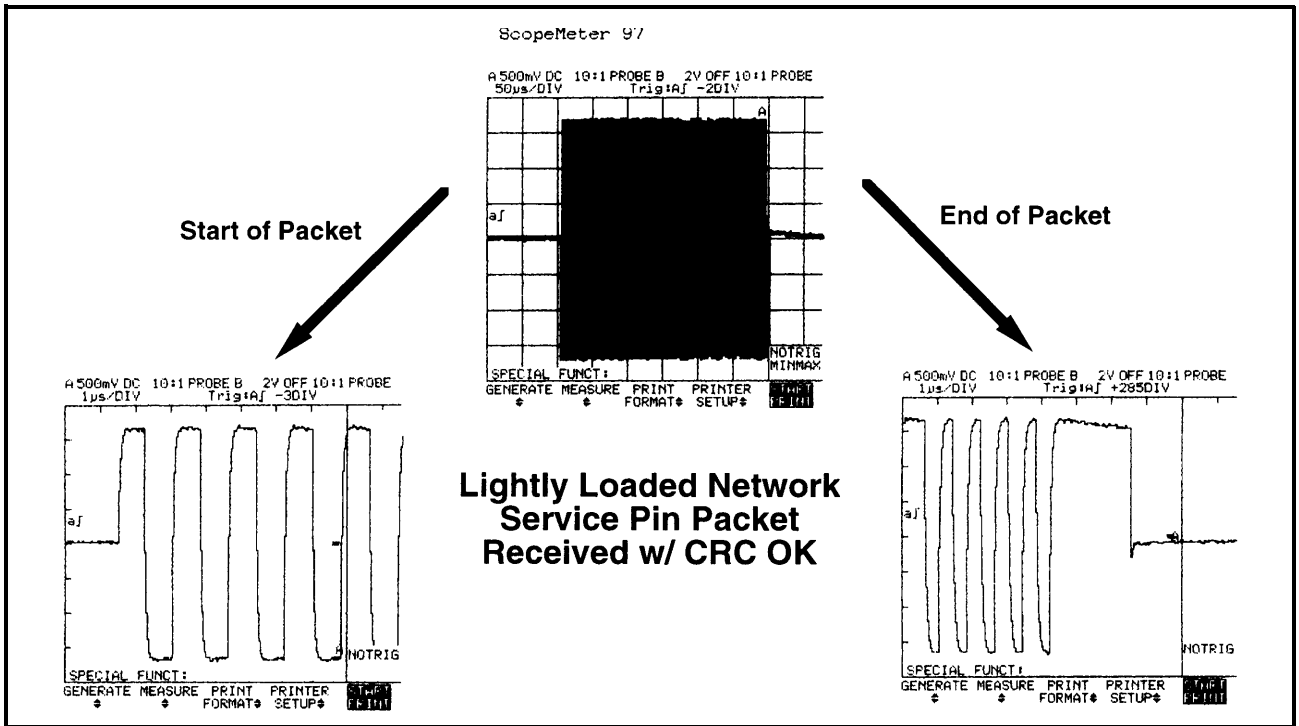
SYMPTOM	POSSIBLE CAUSE
A device cannot communicate on a TP/XF-78 network.	• Use the right-hand side of the Troubleshooting Flowchart shown in [2.] to help in debugging this device's comm problem. First double-check that the wire, connections and termination are correct. Then use Service Pin presses to generate transmit packets, so that the CP line waveforms can be checked [6.1.1]. Another device on the network can be used to generate incoming traffic to the device under test in order to check the CP line waveforms in receive mode. Finally, the analog waveforms on the network can be checked for clues about the lost communication.
A device can communicate on a small network, but not on a large, heavily loaded network.	• Suspect the presence of extra capacitance in the transceiver area, or noise sources on the PC board. Check to be sure that no extra capacitance has been added to the network connection for the device (such as extra transient protection devices like zener diodes). Check also that the PC board layout for the CP lines is low-capacitance (short traces without an adjacent inner-layer ground plane under the traces), Look for noise sources in the 78kbps communication band, like DC-DC converters. If a DC-DC converter is suspected of coupling noise into the transceiver transformer, try re-orienting or moving the inductor to see if communication integrity improves.
When attempting to transmit a packet, the device's CP lines do not behave correctly.	• The TP/XF-78 transceiver uses Differential mode for the CP lines [6.1 .1]. CPO and CP1 are the analog receive lines. CP2 and CP3 are the transmit lines. If the device is incorrectly configured for Single Ended mode or Special Purpose mode, the CP lines will not function correctly.
When a device is powered up and connected to the network, all network communication stops. The device shuts down the whole network.	• Suspect that the comm parameters for this device have been incorrectly set to Special Purpose mode. In Special Purpose mode, CP2 is a "bit clock, " which can toggle at rates in the 78kbps communication band. Since CP2 is normally a transmit data line for the TP/XF-78 transceiver, the bit clock is transmitted (in an attenuated form) onto the network. This waveform can be seen by other devices on the network as a continuous preamble, so those other devices hold off their transmissions waiting for the preamble to stop. If a 3120 Chip is incorrectly loaded with Special Purpose mode comm parameters, it will most likely have to be replaced [5.1 .3]. If a 3150 Chip device is loaded with the wrong comm parameters, it can usually be recovered by using EEBlank [5.2,3].

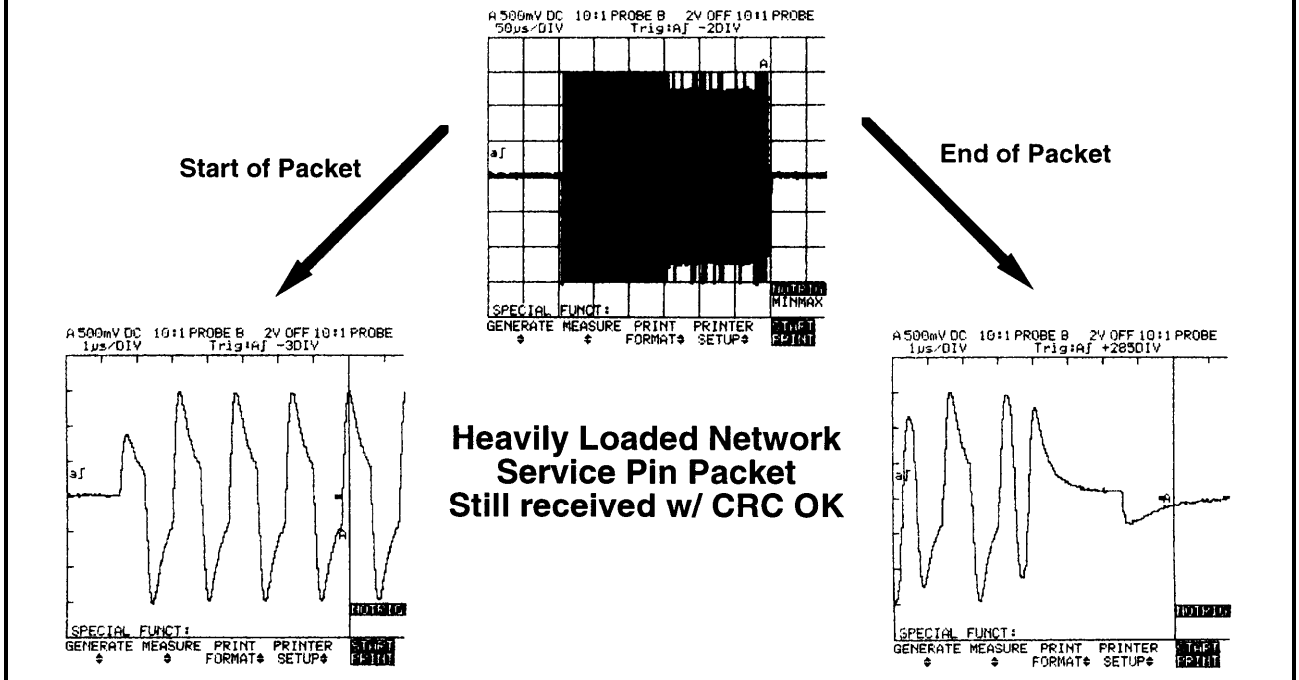
[6.5] Troubleshooting TP/XF-1250 Networks

[6.5.1] Doubly-Terminated Bus Issues

- TP/XF-1250 networks must be wired **in Doubly-Terminated Bus topology.**
- See the TPT User's Guide[6] for detailed information.

[6.5.2] Typical TP/XF-1250 Analog Network Waveforms





[6.5] Troubleshooting TP/XF-1250 Networks (cont.)

[6.5.3] Common Problems with TP/XF-1250 Networks

SYMPTOM	POSSIBLE CAUSE
A device cannot communicate on a TP/XF-1250 network.	• Use the right-hand side of the Troubleshooting Flowchart shown in [2.] to help in debugging this device's comm problem. First double-check that the wire, connections and termination are correct. Then use Service Pin presses to generate transmit packets, so that the CP line waveforms can be checked [6.1.1]. Another device on the network can be used to generate incoming traffic to the device under test in order to check the CP line waveforms in receive mode. Finally, the analog waveforms on the network can be checked for clues about the lost communication.
A device can communicate on a small network, but not on a large, heavily loaded network.	• Suspect the presence of extra capacitance in the transceiver area, or noise sources on the PC board, Check to be sure that no extra capacitance has been added to the network connection for the device (such as extra transient protection devices like zener diodes). Check also that the PC board layout for the CP lines is low-capacitance (short traces without an adjacent inner-layer ground plane under the traces). Look for noise sources in the 1.25Mbps communication band, like DC-DC converters. If a DC-DC converter is suspected of coupling noise into the transceiver transformer, try re-orienting or moving the inductor to see if communication integrity improves.
When attempting to transmit a packet, the device's CP lines do not behave correctly.	• The TP/XF-1250 transceiver uses Differential mode for the CP lines [6.1.1]. CP0 and CP1 are the analog receive lines. CP2 and CP3 are the transmit lines. If the device is incorrectly configured for Single Ended mode or Special Purpose mode, the CP lines will not function correctly.
When a device is powered up and connected to the network, all network communication stops. The device shuts down the whole network.	• Suspect that the comm parameters for this device have been incorrectly set to Special Purpose mode. In Special Purpose mode, CP2 is a "bit clock, " which can toggle at rates in the 1.25Mbps communication band. Since CP2 is normally a transmit data line for the TP/XF-1250 transceiver, the bit clock is transmitted (in an attenuated form) onto the network. This waveform can be seen by other devices on the network as a continuous preamble, so those other devices hold off their transmissions waiting for the preamble to stop. If a 3120 Chip is incorrectly loaded with Special Purpose mode comm parameters, it will most likely have to be replaced [5. 1.3]. If a 3150 Chip device is loaded with the wrong comm parameters, it can usually be recovered by using EEBlank [5.2.3].

[7.] References & Suggested Reading

REFERENCE MATERIALS:

1. *Neuron® Chip Data Book*, available from Motorola & Toshiba.

2. *Neuron C Programmer's Guide*, and *Neuron C Reference Guide*, both available from Echelon Corp.

SOME OF ECHELON'S USER'S GUIDES:

3. *LONWORKS® FTT-10 /10A Free Topology Transceiver User's Guide*.

4. *LONWORKS LPT-10 Link Power Transceiver User's Guide*.

5. *LONWORKS LPI-10 Link Power Interface Module User's Guide*.

6. *LONWORKS TPT Twisted Pair Transceiver Module User's Guide*.

7. *LONWORKS Twisted Pair Control Module User's Guide*.

8. *LONWORKS Router User's Guide*.

9. *LonManager® Protocol Analyzer User's Guide*.

10. *LonBuilder® User's Guide*, and the *NodeBuilder User's Guide*.

SOME OF ECHELON'S ENGINEERING & TECHNICAL BULLETINS:

11. *LONWORKS Custom Node Development* Engineering Bulletin.

12. *Neuron 3150® Chip External Memory Interface* Engineering Bulletin.

13. *Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks*.

14. *LonTalk® Protocol* Engineering Bulletin.

15. *Enhanced Media Access Control with LonTalk Protocol* Engineering Bulletin.

OTHER SOURCES OF USEFUL INFORMATION:

16. Echelon's web site: http://www.echelon.com

17. Echelon's Training Classes: LONWORKS Technology, LNS Network Tools.