LONWORKS®

TPT Twisted Pair Transceiver Module

User's Guide

Revision 3

ECHELON®
Corporation

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Echelon Corporation, Inc.
4015 Miranda Avenue
Palo Alto, CA 94304, USA

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Introduction

The TPT Twisted Pair Transceiver Modules provide a simple, cost effective method of adding a LONWORKS transceiver to any Neuron® Chip-based machine controller, process controller, fire, and security device, or general purpose controller. There are two TPT modules, the TPT/XF-78 and TPT/XF-1250, both of which share a common connector footprint, allowing them to be interchanged without modifying the motherboard PCB hole pattern.

The TPT/XF-78 module consists of a transformer-coupled 78kbps Manchester coded communication transceiver and connectors for power, the Neuron Chip communication port lines, and the two wire network data bus. The TPT/XF-1250 module consists of a transformer-coupled 1.25Mbps Manchester coded communication transceiver and connectors for power, the Neuron Chip communication port lines, and the two wire network data bus.

The TPT modules use a transformer to isolate them from the twisted pair network bus. This design provides excellent common mode rejection, and permits the system to operate in electrically noisy environments. It also reduces the susceptibility of the system to ground loops caused by the use of multiple network power supplies that float relative to ground.

Audience

The *LONWORKS TPT Twisted Pair Transceiver Module User's Guide* provides specifications and user instruction for customers who have purchased TPT modules.

Content

This manual provides detailed technical specifications on the electrical and mechanical interfaces and operating environment characteristics for the transceiver modules.

This document also provides guidelines for migrating applications from a LonBuilder® Developer's Workbench Emulator to a transceiver module-based product design. Complete references are included to simplify the task of integrating the control modules with application electronics.

This document has a list of references in Chapter 7. Whenever a reference document is addressed, a superscript number corresponding to the reference has been placed in the text, i.e., Standler[7]. Whenever a specific chapter or section within a reference has been referred to, the reference is enclosed in brackets and the chapter is addressed by number, i.e., Reference [1], Chapter 8.

Related Documentation

The following Echelon documents are suggested reading:

LonBuilder User's Guide (078-0001-01)

Neuron C Programmer's Guide (078-0002-01)

Neuron C Reference Guide (078-0140-01)

NodeBuilder User's Guide (078-0141-01)

LonBuilder Hardware Guide (078-0003-01)

LONMARK Layers 1-6 Interoperability Guidelines (078-0014-01)

LONMARK Application Layer Interoperability Guidelines (078-0120-01)

Neuron Chip Data Book as published by Motorola and Toshiba

Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks (005-0023-01)

LONWORKS Twisted Pair Control Module User's Guide (078-0015-01)

LONWORKS Custom Node Development (005-0024-01)

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Electrical Interface

The TPT Twisted Pair Transceiver Modules interface to the Neuron 3120 Chip or Neuron 3150 Chip and to the network through two connectors, P1 and P2, respectively. P1 provides access to the transceiver module communication port (CP) pins as well as +5VDC power and ground (see Chapter 4 for power supply requirements). P2 supports connection to the twisted pair data bus.

P1 and P2 Connector Terminals

The pinout of the P1 and P2 connector terminals is shown in tables 2.1 and 2.2. The CP pin function names defined in table 2.1 are identical to the terms used in the *Neuron Chip Data Book*[1] which defines the functions and electrical characteristics for those signal names listed in table 2.1. The CP signals are connected directly to the Neuron Chip without buffering.

Pins 7 and 9 of connector P2 are connected to the twisted pair network. Pin 8, the center tap pin, is normally left open. In some cases, a capacitor between this pin and earth ground can reduce EMI emissions.

Table 2.1 6-Pin Communication Port and Power Supply Connector (P1)

Name	Pin #	Function
CP3	2	See the *Neuron Chip Data Book* for functions.
CP0	3	
CP1	4	
CP2	5	
+5V	6	Power supply input
GND	1	Power supply Ground

Table 2.2 3-Pin Network Connector (P2)

Name	Pin #	Function
CT	8	Transformer center tap
Data	7	Network data B signal
Data	9	Network data A signal

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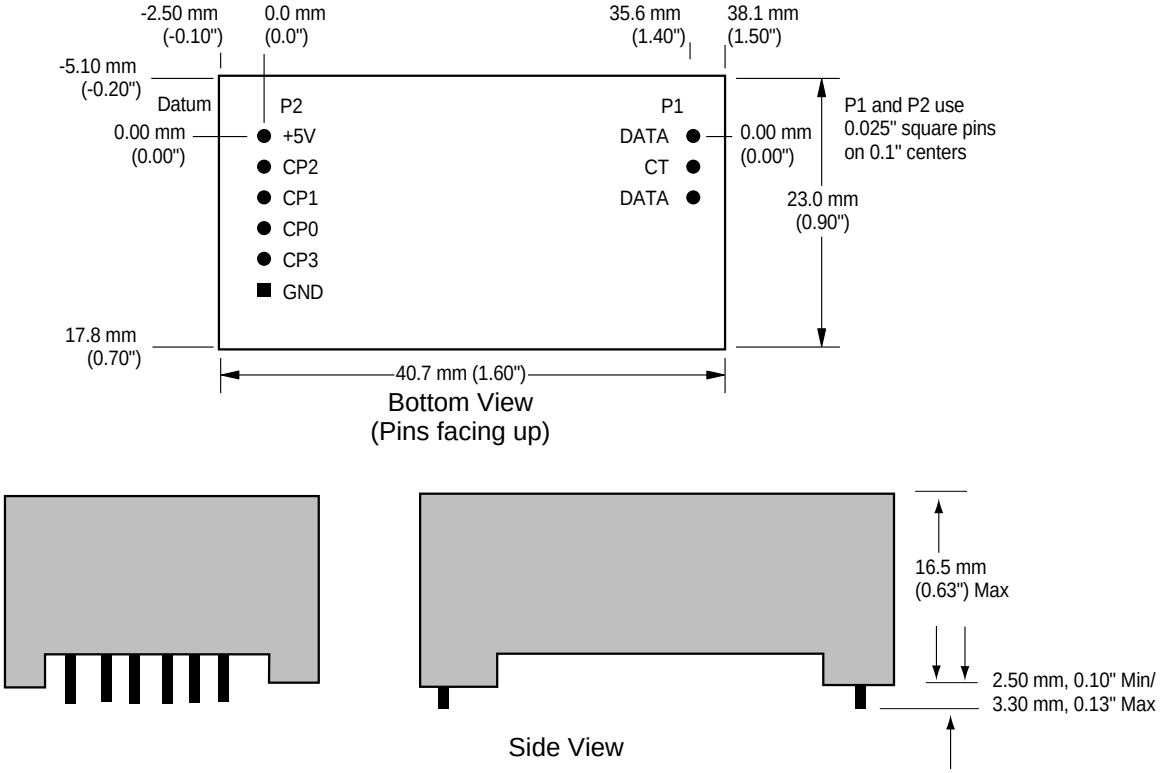
Mechanical Considerations

This chapter discusses the mechanical footprint and connectors of the TPT Twisted Pair Transceiver Modules. Details of mounting to an application electronics board containing a Neuron Chip are provided.

Mechanical Footprint

The TPT Twisted Pair Transceiver Modules footprints and connectors are shown in figures 3.1 and 3.2. The TPT modules are generally mounted to the application board as a thru-hole, soldered component. Decisions about component placement on the application electronics board must also consider electromagnetic interference (EMI) and electrostatic discharge (ESD) issues as discussed in Chapter 6 of this document.

Figures 3.1 and 3.2 also show the maximum height of both the potted and unpotted TPT modules. Application designs using the transformer-coupled twisted pair transceivers should maintain a minimum of 0.15” (3.81mm) clearance from P2 pins and traces on the network side of the transformer to achieve the minimum isolation specified for this module.



All dimensions are ± 0.25 mm, 0.010" unless otherwise stated.

Figure 3.1 Potted TPT Module Mechanical Footprint

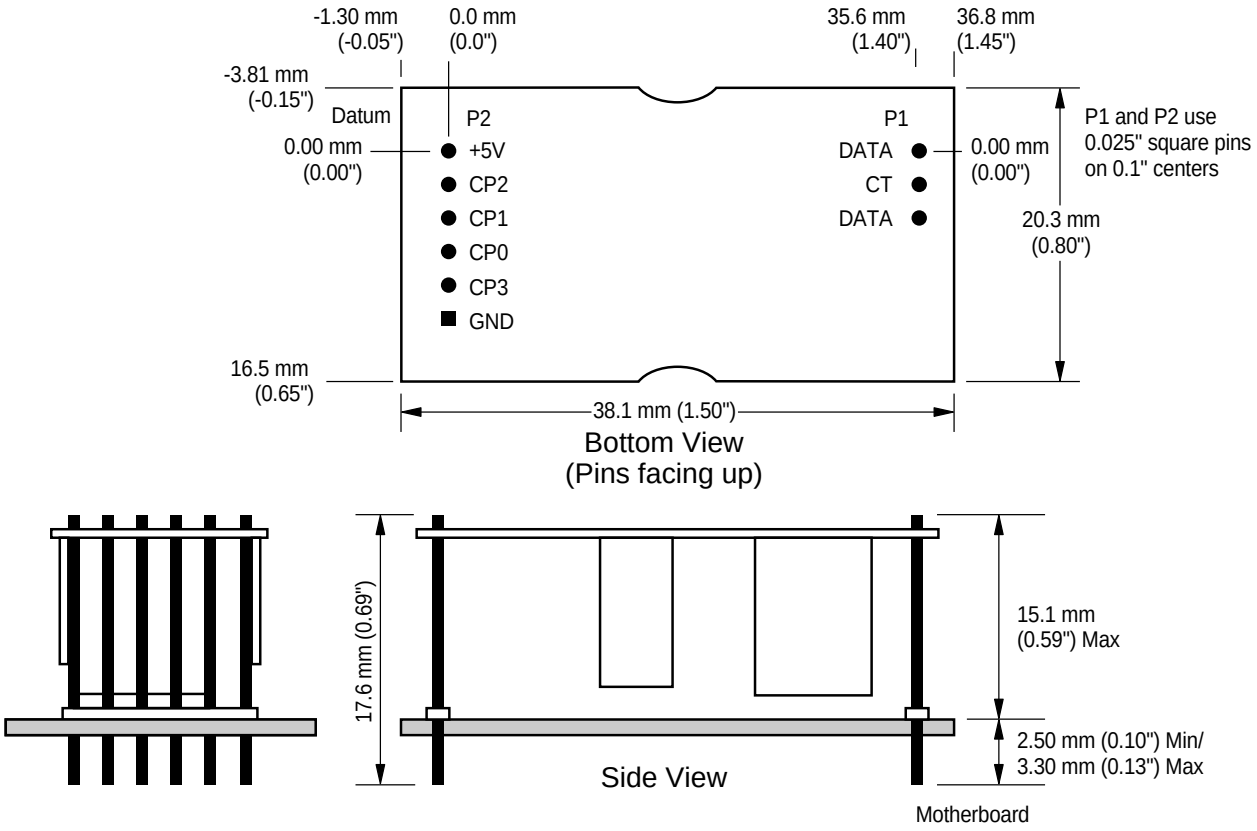


Figure 3.2 Unpotted TPT Module Mechanical Footprint

Note: CP0 and CP1 may be exchanged with one another. CP2 and CP3 also may be exchanged with one another independently of CP0 and CP1. Pins should be exchanged to optimize the PCB layout to eliminate crossovers. See *Designing for Interoperability* in Chapter 6 for additional details regarding PCB layout.

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Power Requirements

This chapter describes the power requirements for the TPT modules as well as considerations for noise filtering in order to comply with both conducted and radiated emissions requirements.

Transceiver Module Power Requirements

The TPT modules require a power source that provides +5VDC±5% at 10mA. The current requirements are characterized for the maximum number of nodes on the channel and the internal isolation relay energized.

Power Supply Decoupling and Filtering

The design of the TPT modules power supply must consider filtering and decoupling requirements of the module. The power supply filter must prevent noise generated by the supply from interfering with module operation. Switching power supply designs must also consider the effects of radiated EMI. The following general guidelines will optimize the performance of the transceiver module:

- Locate at least one (1) 0.1µF multilayer ceramic (MLC) decoupling capacitor next to the power supply pin.
- Inclue a bulk bypass tantalum capacitor of at least 4.7µF somewhere on the application board.
- Use at least two (2) 0.1µF MLCs near the Neuron Chip power supply pins.
- Use one (1) 0.1µF MLC near every other digital IC.
- Keep CP0, CP1 trace lengths as short as possible, and route them well away from digital traces. Use CP2, CP3 as “guard” traces for CP0, CP1.

The TPT modules require a clean power supply to prevent RF noise from conducting onto the network through their coupling circuits. Power supply noise at a frequency close to the network transmission frequency may degrade network performance.

Attention to the design of the application electronics circuit is also necessary. High-speed signals and inductive loads are common sources of noise which must be managed by separating the logic and I/O power supplies, or by using sufficient filtering and decoupling techniques.

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Network Cabling and Connection

This chapter provides information about cabling and connections for the TPT modules. This information includes a discussion of wire characteristics and bus terminations.

Performance Characteristics

The number of nodes per channel and the length of the bus cabling are dependent on temperature. Table 5.1 summarizes these parameters. The worst case cable distances take into account variations in node distribution, node temperature, node voltage, wire characteristics, transceiver characteristics, and Neuron Chip characteristics, and allow for an average cable temperature of up to +55° C. The wire characteristics and type are described in the table.

Table 5.1 Performance Characteristics

Transceiver Type	*Number of Nodes*	*Temperature*	*Worst Case Bus Length*	*Maximum Stub Length*
TPT/XF-78	64	0 to +70°C	1400m (4600 feet)	3m (9.8 feet)
TPT/XF-78	44	-40 to +85°C	1400m (4600 feet)	3m (9.8 feet)
TPT/XF-1250	64	0 to +70°C	130m (430 feet)	0.3m (12 inches)
TPT/XF-1250	32	-20 to +85°C	130m (430 feet)	0.3m (12 inches)
TPT/XF-1250	16	-40 to +85°C	130m (430 feet)	0.3m (12 inches)

Wire Characteristics

The TPT modules are designed for distributed control applications using low-cost, Level IV twisted pair wire. The characteristics of the wire used to implement a network will affect the overall system performance with respect to total distance, stub length, and total number of nodes supported on a single channel. The TPT transceivers have been qualified using **only** Level IV, 22 AWG (0.65mm) twisted pair cable for the primary bus, and either Level IV, 24AWG (0.5mm) or Level IV, 22AWG cable for stubs. Under no circumstances should smaller gauge Level IV cable be substituted for Level IV, 22 AWG (0.65mm) twisted pair cable for the bus, or should Category IV cable be used in lieu of Level IV cable. Echelon periodically qualifies new cables for twisted pair transceivers, and it is advisable to check with Echelon from time to time to determine if new cables are available for the TP-78 and TP-1250 channels.

The characteristics and suppliers of Level IV cable are described in the document *Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks*[9] (Echelon part 005-0023-01).

Node Distribution Rule for TP/XF-1250 Segments

Due to the transmission characteristics of the TP-1250 channel, communication failures may result from reflections of the TPT/XF-1250 transceiver's 1.25Mbps transmitted signal under conditions of concentrated node loading. These communication failures are eliminated when nodes are used in a distributed

configuration. For this reason, it is essential to follow a simple topology rule when using TPT/XF-1250 transceivers and/or TP/XF-1250 control modules and/or TPM-1250 SMX transceivers to eliminate the possibility of reflection-related transmission failures. **No such topology rule applies to the use of TPT/XF-78 transceiver, TP/XF-78 control modules, or TPM-78 SMX transceivers.**

Referred to as the "8-in-16" topology rule, this rule requires that no more than 8 TP/XF-1250 Control Modules and/or TP/XF-1250 Transceivers and/or TPM-1250 SMX Transceivers be located within any 16 meter length of cable. This means that no matter where along the bus the 16 meter measurement is taken, there should be no more than 8 nodes. Figure 5.1 provides a diagram of such a measurement technique.

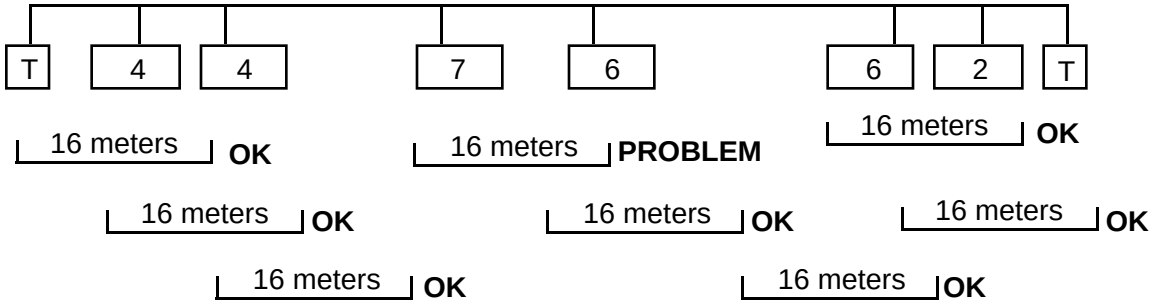


Figure 5.1 8-in-16 Topology Rule Example

In the example we see an installation with six groups of nodes, varying in size from 2 to 8 devices, in a doubly terminated bus. By using a 16 meter measurement stick that we can move from side-to-side over the length of the bus, we can determine whether the 8-in-16 rule has been met (designated by the word "OK") or violated (shown by the designation "PROBLEM"). In the case of the PROBLEM area, a total of 13 nodes are located within a 16 meter length of the bus, which amounts to five more nodes than are permitted under the 8-in-16 rule.

There are two solutions that can be applied to situations in which the 8-in-16 rule has been, or must be, violated by virtue of the installation scenario. The first and simplest remedy is to insert a router and two termination networks in the bus to break the network into two channels (figure 5.2). Since each side of the router comprises a different channel, the bus is effectively split and the nodes divided between two channels.

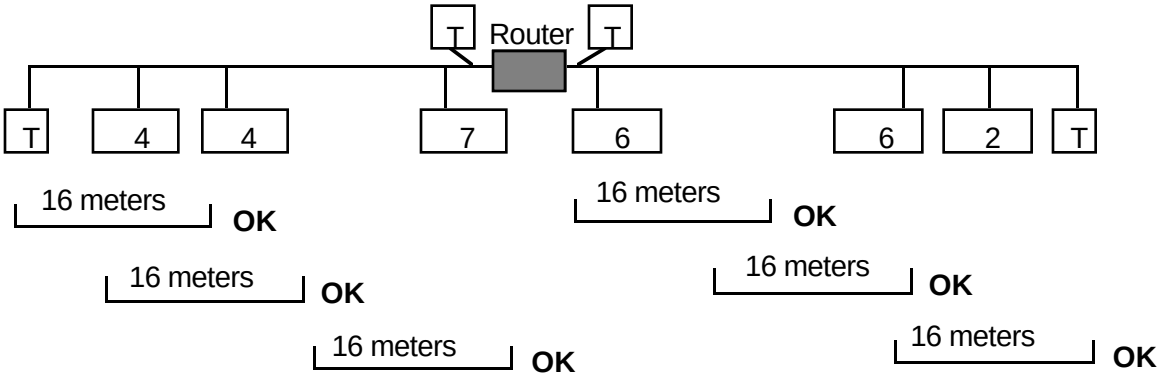


Figure 5.2 Using a Router to Meet the 8-in-16 Topology Rule

The second remedy to a violation of the 8-in-16 rule is to add additional cable to the bus such that the rule is no longer violated (figure 5.3). It is important to ensure that the maximum bus length (130 meters of 22AWG/0.65mm Level IV twisted pair) is not exceeded by the additional cable. Due to the complex interactions between the bus and the transceivers with regard to reflections and transmission line delays, it is not possible to substitute an LC network in lieu of the additional cable to resolve this rule violation.

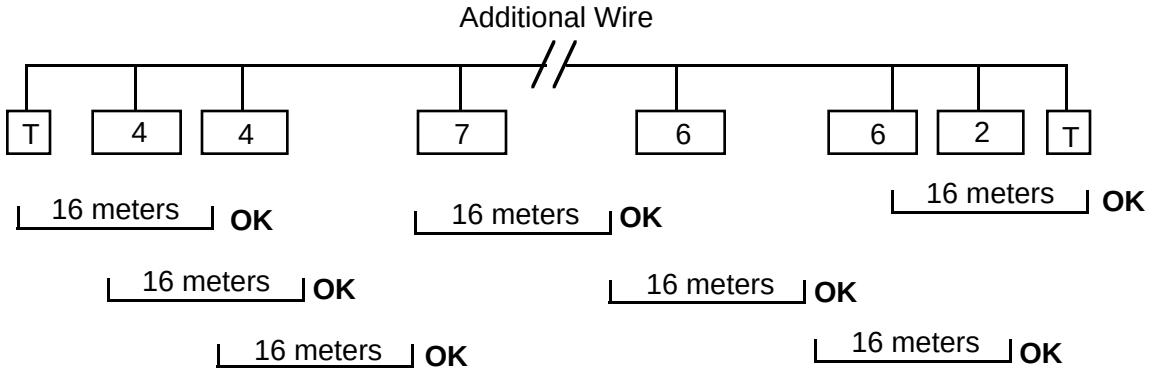
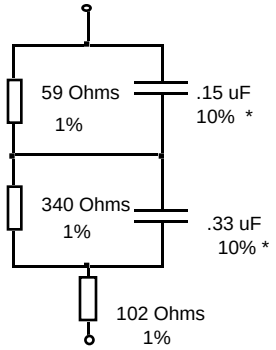


Figure 5.3 Using Additional Bus Cable to Meet the 8-in-16 Topology Rule

Bus Termination

It is necessary to terminate both endpoints of the twisted pair bus for proper data transmission performance. Failure to terminate the bus will degrade network performance. Figure 5.4 shows the circuit required to terminate a twisted pair bus.



* Capacitors are metal polyester, 50V

Figure 5.4 Required Bus Termination for Twisted Pair Networks

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Design Issues

This chapter looks at design issues and includes a discussion of Electromagnetic Interference (EMI), and Electrostatic Discharge (ESD), and Designing for Interoperability.

EMI Design Issues

The high-speed digital signals associated with microcontroller designs can generate unintentional Electromagnetic Interference (EMI). High-speed voltage changes generate RF currents that can cause radiation from a product if a length of wire or piece of metal can serve as an antenna.

Products that use the TPT modules together with a Neuron Chip will generally need to demonstrate compliance with EMI limits enforced by various regulatory agencies. In the USA, the FCC[3] requires that unintentional radiators comply with Part 15 level "A" for industrial products, and level "B" for products that can be used in residential environments. Similar regulations are imposed in most countries throughout the world[4,5].

Designing Systems for EMC (Electromagnetic Compatibility)

Careful design of application electronics is important to guarantee that TPT module-based nodes will achieve the desired EMC. Information on designing products for EMC is available in several forms including books,[6] seminars, and consulting services. This section provides useful design tips for EMC.

EMC Design Tips

- Most of the RF noise originates in the Neuron Chip portion of the TPT module-based nodes, and in any high-frequency or high-speed application circuitry in the node.
- Most of the EMI will be radiated by the network cable and the power cable.
- Filtering is generally necessary to keep RF noise from getting out on the power cable.
- The TPT modules must be well grounded within the nodes to ensure that their built-in EMI filtering works properly.
- Early EMI testing of prototypes at a certified outdoor range is an extremely important step in the design of level "B" products. This testing ensures that grounding and enclosure design questions are addressed early enough to avoid most last-minute changes (and their associated schedule delays).

ESD Design Issues

Electrostatic Discharge (ESD) is encountered frequently in industrial and commercial use of electronic systems[7]. Reliable system designs must consider the effects of ESD and take steps to protect sensitive components. Static discharges occur frequently in low-humidity environments when operators touch electronic equipment. The static voltages generated by humans can easily exceed 10kV. Keyboards, connectors, and enclosures provide paths for static discharges to reach ESD sensitive components such as the Neuron Chip. This section describes techniques for designing ESD immunity into TPT module-based products.

Designing Systems for ESD Immunity

ESD hardening includes the following techniques:

- Provide adequate creepage and clearance distances to prevent ESD hits from reaching sensitive circuitry;
- Provide low impedance paths for ESD hits to ground;
- Use diode clamps or transient voltage suppression devices for accessible, sensitive circuits

The best protection from ESD damage is circuit inaccessibility. If all circuit components are positioned away from package seams, the static discharges can be prevented from reaching ESD sensitive components. There are two measures of "distance" to consider for inaccessibility: creepage and clearance. Creepage is the shortest distance between two points along the contours of a surface. Clearance is the shortest distance between two points through the air. An ESD hit generally arcs farther along a surface than it will when passing straight through the air. For example, a 20 kV discharge will arc about 10 mm (0.4 inches) through dry air, but the same discharge can travel over 20mm (0.8 inches) along a clean surface. Dirty surfaces can allow arcing over even longer creepage distances.

When ESD hits to circuitry cannot be avoided through creepage, clearance, and ground guarding techniques, i.e., at external connector pins, explicit clamping of the exposed lines is required to shunt the ESD current. Consult Standler[7] for advice about ESD and transient protection for exposed circuit lines. In general, exposed lines require diode clamps to the power supply rails or Zener clamps to chassis ground in order to shunt the ESD current to ground while clamping the voltage low enough to prevent circuit damage.

It is recommended that two pairs of clamp diodes be placed on the CP lines between the transceiver module and the Neuron Chip as shown in figure 6.1. The 0.1µF capacitor and diodes should be placed as close as possible to the transceiver module.

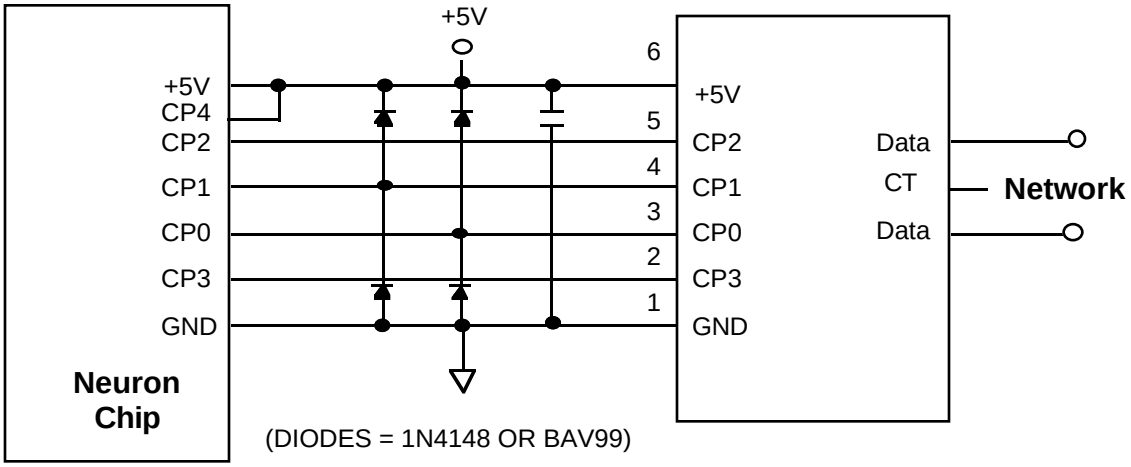

Figure 6.1 ESD Clamps on CP Lines

Designing for Interoperability

In order to meet the LONWORKS interoperability guidelines for transformer-coupled nodes, the mutual capacitance of data pair conductors (differential capacitance) from the twisted pair medium tap connector to the connector which mates to the TPT module P1 header must be kept below 5pF for 78kbps modules, and below 2pF for the 1.25Mbps modules. To meet this requirement, PCB trace lengths between the TPT module P1 and the node medium tap connectors should be kept to less than 5 cm for 78kbps modules, and less than 2 cm for 1.25Mbps modules.

To achieve shielding and minimize capacitance, symmetrical layout guidelines must be followed for the communications port traces connecting the TPT module with the Neuron Chip.

In figure 6.1, note that the two electrically sensitive receive traces, CP0 and CP1, are shielded by the transmit traces CP3 and CP2. When routing CP traces from the Neuron 3150 Chip it is recommended that CP3 (pin 31) be routed directly underneath the Neuron Chip via the NC pin (pin 27) to achieve symmetry and shielding of the traces from the Neuron Chip to the module. To eliminate crossovers, CP0 and CP1 may be exchanged with one another. CP2 and CP3 also may be exchanged with one another independently of CP0 and CP1. This will prove especially useful when routing CP traces between the Neuron 3120 Chip and the module. The total trace distance between the Neuron Chip CP pins and the module must be less than 2 cm (0.8”).

The mutual (differential) capacitance between CP0-CP1 traces must be kept below 3pF for both the TPT/XF-78 and TPT/XF-1250 modules. To meet this requirement, PCB trace lengths between the TPT module P1 connector and the Neuron Chip should be less than 3 cm.

7

References

This section provides a list of the reference material used in the preparation of this manual. See Echelon's World Wide Web site (`http://www.lonworks.echelon.com`) for the latest versions of Echelon's engineering bulletins.

Reference Documentation

[1] *Neuron Chip Data Book*, Motorola, or Toshiba.

[2] *LONWORKS Custom Node Development* engineering bulletin, Echelon Corporation.

[3] 47CFR15, Subpart B (Unintentional Radiators), *U.S. Code of Federal Regulations*, (formerly known as FCC Part 15, Subpart J).

[4] *VDE 0871*, Class "B", tested per VFG1046/1984.

[5] *EN55022*, new EC EMC Standard.

[6] *Noise Reduction Techniques in Electronic Systems*, 2nd ed., by Henry W. Ott, John Wiley & Sons, 1988.

[7] *Protection of Electronic Circuits from Overvoltages*, by Ronald B. Standler, John Wiley & Sons, 1989.

[8] *Electromagnetic Compatibility for Industrial-Process Measurement and Control Equipment, Part 2: Electrostatic Discharge Requirements*, IEC 801-2, 1991-04, draft.

[9] *Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks* engineering bulletin (005-0023-01), Echelon Corporation.