ECHELON®

Pyxos FT Chip Data Book

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Welcome

Echelon's Pyxos™ FT Chip is the network transceiver for the Pyxos FT embedded I/O bus platform. The Pyxos FT Chip facilitates development of high-speed, low-cost, embedded control networks and sensor networks.

This document provides detailed technical specifications for the electrical and electronic interfaces, mechanical interfaces, and operating environment characteristics for the Pyxos FT Chip. In some cases, example vendor sources are included to simplify the task of integrating the Pyxos FT Chip with application electronics. You can find contact information for the vendor sources listed in Appendix C, *Vendor Contact Information*, on page 101.

Except where specified otherwise, the term *Pyxos* in this document refers to Pyxos FT technology.

Audience

This manual provides specifications and user instructions for engineers who develop applications and devices that use the Pyxos FT Chip.

Related Documentation

In addition to the *Pyxos FT Chip Data Book*, the following manuals describe the Pyxos platform:

- *Introduction to the Pyxos FT Platform*. This manual introduces the concepts, technology, and tools for the Pyxos FT platform.
- *Pyxos FT Programmer's Guide*. This manual describes the API for the Pyxos FT platform, how to use the API to develop applications that use the Pyxos FT platform, and how to program directly to the Pyxos FT Chip when you cannot use the API.

The following manuals describe the Pyxos FT EVK Evaluation Kit:

- *Pyxos FT EVK Quick Start Guide*. This guide helps you set up and install the Pyxos FT EVK Evaluation Boards and helps you get started with the Pyxos FT EVK examples. A printed copy of this guide is included with the Pyxos FT EVK.
- *Pyxos FT EVK User's Guide*. This manual describes Pyxos FT EVK hardware, how to assemble the hardware, and how to use the hardware and software that is included with the Pyxos FT EVK to demonstrate Pyxos FT technology and to develop your own Pyxos Pilots and Points.

In addition to the Pyxos FT platform manuals, the following manuals can also be useful for Pyxos FT development projects and are available from the Echelon Web site (www.echelon.com):

- *Introduction to the LONWORKS System.* This manual provides an introduction to the ANSI/EIA/CEA-709.1 (EN14908) Control Networking Protocol, and provides a high-level introduction to LONWORKS® networks and the tools and components that are used for developing, installing, operating, and maintaining them.
- *ShortStack User's Guide*. This manual describes how to develop applications for LONWORKS devices that use the ShortStack® Micro Server. It also describes the architecture of a ShortStack device and how to develop one.

- *LONWORKS Host Application Programmer's Guide*. This manual describes how to create LONWORKS host applications. Host applications are application programs that run on hosts other than Neuron® Chips and use the LONTALK® protocol to communicate with devices on a LONWORKS network.

When you install the Pyxos FT EVK, you can view all of the Pyxos FT platform documents from the Windows® **Start** menu: select **Programs → Echelon Pyxos FT EVK → Documentation,** then select the document that you want to view. They are also available from the Echelon Web site.

All of the Pyxos FT platform documentation, and related-product documentation, is available in Adobe® PDF format. To view the PDF files, you must have a current version of the Adobe Reader®. The Pyxos FT EVK CD includes the English-language version of the Adobe Reader; you can download other language versions from Adobe at: www.adobe.com/products/acrobat/readstep2.html.

Standards Documents Referenced in this Manual

This manual refers to the following standards documents:

- Comité européen de normalisation electrotechnique[1] (CENELEC) EN 55022 – Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement.
- Comité international spécial des perturbations radioélectriques[2] (CISPR) 22 – Information Technology Equipment – Radio Disturbance Characteristics – Limits and Methods of Measurement.
- Electrostatic Discharge Association standard ESD STM5.1: Electrostatic Discharge Sensitivity Testing – Human Body Model. www.esda.org/freedowloads.html
- European Union Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC. europa.eu.int/eur-lex/pri/en/oj/dat/2003/l_037/l_03720030213en00190023.pdf
- International Electrotechnical Commission (IEC) Electromagnetic Compatibility (EMC) standards (see **Table 1** on page v).
- Institute for Printed Circuits (IPC) / Joint Electron Device Engineering Council (JEDEC) Solid State Technology Association standard: IPC/JEDEC J-STD-020C – Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices. www.jedec.org/download/search/jstd020c.pdf
- Title 47 of the Code of Federal Regulations (CFR) Part 15, Radio Frequency Devices. www.fcc.gov/oet/info/rules/
- US Military Standard MIL-STD-883 Test Method Standard, Microcircuits: Method 3015.7, Electrostatic Discharge Sensitivity Classification.

You can purchase copies of CENELEC documents, IEC EMC standards, US Military Standards, and CISPR documents from the Information Handling Services (IHS) Global page at: global.ihs.com.

[1] European Committee for Electrotechnical Standardization

[2] International Special Committee on Radio Interference

Table 1. IEC Electromagnetic Compatibility (EMC) Standards

Standard	Title
IEC 61000-4-2	Electromagnetic Compatibility (EMC) - Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test
IEC 61000-4-3	Electromagnetic Compatibility (EMC) - Part 4-3: Testing and Measurement Techniques – Radiated, Radio-Frequency, Electromagnetic Field Immunity Test
IEC 61000-4-4	Electromagnetic Compatibility (EMC) - Part 4-4: Testing and Measurement Techniques – Electrical Fast Transient/Burst Immunity Test
IEC 61000-4-5	Electromagnetic Compatibility (EMC) - Part 4-5: Testing and Measurement Techniques – Surge Immunity Test
IEC 61000-4-6	Electromagnetic Compatibility (EMC) - Part 4-6: Testing and Measurement Techniques – Immunity to Conducted Disturbances, Induced by Radio-Frequency Fields

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1

Introduction

This chapter introduces the Pyxos FT Chip and describes some of the benefits of Pyxos FT technology.

Product Overview

The Pyxos FT platform is Echelon's platform for embedded control networks. You can use the Pyxos FT platform to develop smart devices and controllers that communicate with remote sensors and actuators. You can use a Pyxos FT network as a low-cost, high-performance sensor and actuator I/O bus that extends the reach of any control system or control network to a wide variety of sensors and actuators.

You can also use the Pyxos FT platform to replace existing wiring harnesses, or more expensive solutions, with a simple twisted-pair cable. Embedded control networks based on the Pyxos FT platform can reduce costs for product installation, warranty, and total life-cycle.

The Pyxos FT Chip is a simple, small, low-cost component that enables the development of Pyxos FT embedded control-networking applications. The Pyxos FT Chip acts as the transceiver for managing communications on the Pyxos FT network, and it embeds the communications protocol for the Pyxos FT platform.

A Pyxos FT network consists of one master device, called the *Pilot*, that manages Pyxos FT network communication. The Pilot is typically the network controller, but it can also act as a gateway for other networks, such as LONWORKS networks. A Pyxos FT network also includes one or more subordinate devices, called *Points*, that perform distributed I/O functions and communicate with the Pilot. A Pyxos FT network can support up to 32 Points. The Pyxos FT platform uses the same data types as the LONWORKS platform, which provides seamless integration of Pyxos Points with LONWORKS devices, and enables multiple Pyxos FT networks to use a LONWORKS network as the backbone.

Pyxos FT devices use the Pyxos FT Chip to communicate with other Pyxos FT devices over a shared twisted-pair cable that you can configure as a bus or as a free-topology network. The Pyxos FT Chip performs signal processing that allows communications over long distances and in noisy environments. The Pyxos FT Chip includes a built-in protocol engine that provides deterministic and reliable data delivery.

The Pyxos FT EVK Evaluation Kit is a set of hardware and software tools that you can use to demonstrate the functions and capabilities of Pyxos FT platform and to develop your own devices that incorporate Pyxos FT technology. The Pyxos FT EVK product includes the Pyxos FT application programming interface (API) and the Pyxos FT Interface Developer utility that work with standard development tools for your selected host microprocessor to provide a simple means for configuring and developing applications for the Pyxos FT Chip.

Built-In Protocol

A Pyxos FT system is comprised of a Pilot and up to 32 Points. The Pilot receives data from the Points and sends control information to the Points. The Points perform distributed I/O functions; they collect sensor data and control actuator outputs for the system.

The Pyxos Pilot and Pyxos Points on a Pyxos FT network communicate using a common communications protocol called the *Pyxos FT protocol*. The Pyxos FT protocol uses time-division multiplexing (TDM) to manage the communications between the Pilot and the Points. The protocol encodes multiple simultaneous bit streams as sub-channels in a single bit stream. The different sub-channels are the bit streams from the different Points on the Pyxos FT network, each communicating with the Pilot. Each of the sub-channels has a fixed bit rate, which provides deterministic response for each of the sub-channels. The Pyxos FT Chips on the Pilot and the Points manage the interleaving of the channels.

The Pyxos FT protocol divides the time domain for the bit streams into several recurrent *timeslots* of fixed length. There is one timeslot for each sub-channel. A Pyxos *frame* consists of a window of time that contains all of the timeslots for all of the sub-channels. Each frame includes eight bytes of data sent from the Pilot to each Point, and another eight bytes of data sent from the each Point to the Pilot.

A Pilot and its Points exchange data using a data abstraction called a *Pyxos network variable* (*PNV*). A PNV has a direction (Pilot-to-Point or Point-to-Pilot), size (1 to 32 bytes), type, and format. The PNV type specifies the encoding, units, resolution, scaling, and structure for the PNV value. A rich set of more than 180 *standard network variable types* (SNVTs) is defined for the Pyxos platform. These types are shared with the LONWORKS platform, thus providing seamless interfaces from Pyxos sensors and actuators to LONWORKS devices.

The Pyxos FT protocol ensures reliable delivery of data. The protocol engine automatically handles transaction acknowledgements, and new data cannot be sent until the previous data has been successfully received. Each packet has its own 18-bit cyclic redundancy check (CRC) value for error detection so that only valid data is delivered and acknowledged. And the Pyxos FT Chip physical layer transceiver employs sophisticated signal processing algorithms to ensure reliable communications in extremely noisy environments.

For more information about the Pyxos FT protocol, see the *Introduction to the Pyxos FT Platform* and the *Pyxos FT Programmer's Guide*.

Link Power

The Pyxos FT Chip can share the communication medium with 24 V AC or DC power. This sharing allows for a simple power distribution scheme with a centralized 24 V source power supply that distributes the power over the twisted-pair wire to each of the Pyxos FT devices. Each Pyxos FT device on the network can then regulate the 24 V to a local supply voltage for its own power requirements. In some cases, the device can use a simple linear power supply; devices that require more power can use a switching power supply.

For more information about link power, see Chapter 6, *Link Power*, on page 53.

Ease of Use

The Pyxos FT Chip allows you to create systems that are easy to install and maintain. Because Pyxos FT networks are self-organizing, both installation time and equipment costs can be reduced by eliminating the need for specialized skills or special tools for network installation.

With self-organization, after a device has been attached to the network, installation can be as simple as turning on the power. The Pyxos FT Chip supports automatic device registration with the network: when it is powered on, the device waits for an available timeslot on the network and notifies the Pilot of its presence. The Pilot can then configure the device appropriately. Other device registration methods are also supported – such as taking network configuration information from a wiring harness or manually with the press of a button.

Echelon's polarity-insensitive free topology technology, together with self organization, allows devices to be attached to the network in a way that is convenient for the installer. As long as he or she does not exceed the network distance limits, the installer can be confident that the system will operate, without being restricted to a bus topology or being concerned with wiring errors.

Scalability

The Pyxos FT Chip is designed to operate in a wide range of applications, from inside-the-box communications to entire buildings. The Pyxos FT Chip can operate in environments with high electrical noise, such as those found in many industrial settings. In addition to these features, the Pyxos FT Chip is inexpensive to use and has special features that minimize the need for external circuitry.

A Pyxos FT network can be up to 400 m for a doubly terminated bus or up to 100 m for a singly terminated free-topology network, and can contain from one to 32 Points. The TDM frame time scales with the number of timeslots on the network, from 25 ms for a network with 32 timeslots defined to less than 2 ms for a small network with just two timeslots defined. You can run the protocol at a slower rate to reduce processing requirements and power consumption in systems that do not require fast response time.

The Pyxos FT Chip supports low-cost external passive components for network coupling to provide significant noise immunity and electrical isolation. This can range from no additional coupling components for enclosed systems, to transformer isolation for industrial applications, with several options in between. The network coupling circuits use small, inexpensive capacitors, inductors, and an optional transformer. The simplest coupling method adds no cost to a Pyxos FT device, and even the most robust of the recommended coupling circuit designs adds only a small fraction of the cost of the Pyxos FT Chip.

A hosted Pyxos FT device can use almost any microprocessor or microcontroller. Some applications, such as a Pilot or a hosted Point with complicated I/O requirements, benefit from a higher performance microprocessor, such as an ARM7 family processor. Others, such as a simple hosted Point with only a few I/O, can use an inexpensive eight-bit microprocessor with limited hardware resources, such as an AVR microprocessor. Or a Pyxos FT Point can be unhosted, using no microprocessor, using the Pyxos FT Chip's built-in digital I/O.

Development Resources

Many resources are available to facilitate device and system development with the Pyxos FT Chip, including resources to assist in developing hardware and software.

The Pyxos FT API is an ANSI C API that provides easy-to-use functions that can be called by Pilot and Point applications to send and receive data between the Pilot and Points using the Pyxos FT protocol. The Pyxos FT Interface Developer utility provides a simple means for configuring Pilot and Point applications and for creating descriptions of the interfaces that the applications use.

The Pyxos FT EVK provides example hardware and software that demonstrate many of the critical features and benefits of the Pyxos FT Chip and of Pyxos FT networks. The EVK includes three Points and a Pilot, with all of the Points running with link power supplied by the Pilot. The EVK includes an unhosted Point, a hosted Point based on a low-cost AVR microprocessor, and a hosted Point based on a higher-performance ARM7 microprocessor. The Pilot also includes a LONWORKS Gateway that provides optional communication with LONWORKS networks or devices. The EVK includes a visualization tool, the Pyxos Network Example HMI application program, that provides interaction with the Points and Pilot from a Windows computer.

The rest of this manual provides detailed descriptions of how to design Pyxos FT devices and systems. For an introduction to the Pyxos FT platform, see the *Introduction to the Pyxos FT Platform*. For firmware development information, including the Pyxos FT API, see the *Pyxos FT Programmer's Guide*. For information about the Pyxos FT EVK, see the *Pyxos FT EVK User's Guide*.

Interoperability with LONWORKS Networks

You can design a Pyxos Pilot so that it can connect to a LONWORKS network. This interoperability allows you to create systems that leverage the strengths of the two complementary platforms. The Pyxos FT platform is ideal for controller-to-remote-I/O communication leveraging its deterministic data delivery, very fast response times, and easy support of third-party microcontrollers. The LONWORKS platform is ideal for controller-to-controller and controller-to-workstation communication leveraging its peer-to-peer network communications, scalability to tens of thousands of devices, sophisticated network management tools, and an integrated microprocessor that is designed to fulfill the needs of control applications.

The combination of Pyxos FT networks and LONWORKS networks provides greater benefits than either technology can on its own. LONWORKS networks connect controllers and machines together to create control and monitoring applications, while Pyxos FT networks can reside around those controllers and inside those machines, and thus extend the reach of your LONWORKS applications to the smallest sensor or actuator device.

A Pyxos Pilot can communicate with a LONWORKS network by using an Echelon Smart Transceiver with Echelon's ShortStack® Micro Server and ShortStack API. Complex Pilots can use a Smart Transceiver with Echelon's Microprocessor Interface Program (MIP) firmware and host API. In either case, the Pilot application can expose some or all of the Pyxos network variables (PNVs) as LONWORKS network variables, which allows for seamless application integration.

LONWORKS network variables representing PNV values can use the same network variable types as the PNVs that they represent. LONWORKS network variables that represent calculated values or other conditions can use different network variable types. The Pilot application might even provide for configuration of the Pyxos FT system through LONWORKS network variable, which can make controlling Pyxos FT networks easy and affordable. The Pyxos FT system would then appear as a single LONWORKS device that enjoys the full privileges of membership in a LONWORKS network.

Together, LONWORKS devices and Pyxos FT devices increase the power of standalone LONWORKS and Pyxos FT networks, and provide end users with more detailed and accurate monitoring, service, and control of devices. LONWORKS and Pyxos FT networks create a synergistic system, with LONWORKS providing the ultra-reliable backbone for any number of Pyxos FT-based controllers, machines, and sensor-actuator networks.

2

Pyxos FT System Design Principles

This chapter introduces the more important design principles for Pyxos FT systems, networks, and devices.

Pyxos FT System Design

Because a Pyxos FT device is a combination of hardware resources and firmware resources, as a Pyxos FT device designer, you have a number of system-level decisions to make that can affect overall system performance, communications performance, power distribution and usage, electromagnetic compatibility (EMC), system reliability, system interoperability with other devices, product size, product manufacturing cost, and other factors.

This chapter provides an overview of the more important system, hardware, and firmware design decisions that you need to make when developing a Pyxos FT system.

System Design Considerations

At a high level, system design for Pyxos FT devices includes many of the same design considerations as do other embedded and networking devices, such as:

- How are system functions partitioned?
- Does the system have an open or closed architecture?
- Is the system primarily static or primarily dynamic?
- How will the system be maintained?
- What level of interoperability with other Pyxos FT devices and other systems is required?

As with most design decisions, the answers to each of these questions requires you to decide which side of a trade-off is most appropriate for your system.

Functional Partitioning

There are two basic types of functional partitioning for a Pyxos FT system:

- Location-based partitioning
- Function-based partitioning

For location-based partitioning, a single Point handles all of the system functionality for a particular geographic location. For example, a Point could handle all of the room-control functions (lighting, temperature, humidity, and so on) for a single room. Other Points would handle these same functions for other rooms.

For function-based partitioning, a single Point handles one (and usually only one) function for a particular system. For example, a Point could handle only the light-level-monitoring function for a room-controller network. Other Points would handle other functions for the network; thus, you could have one Point for light-level monitoring, another for controlling the lamps, another for processing switch inputs, and so on.

A single system could include elements of both types of partitioning. For example, you could have a function-based system for handling the lighting for a room-control network (including the light sensors, switches, and lamps), and a location-based partition for temperature control so that the temperature sensors and control system are local to each room within the network.

How you partition the overall system functionality can impact other system-design considerations, such as system performance (how much data does a particular Point have to process during a particular period of time?), communications performance (if the Point

cannot send all of its data in one network frame, how long can the system wait to receive all of the Point's data?), power distribution and usage (a Point that performs many functions will likely require more power than a Point that performs fewer functions), and so on.

System Architecture: Open or Closed

The architecture for a Pyxos FT system can be basically open or basically closed. An open architecture is one in which a device performs general functions and has no prior knowledge of the system in which it performs these functions. A closed architecture is one in which a device performs specialized functions and possibly has prior knowledge of the system in which it performs these functions (such as, specific knowledge of the other devices with which it interoperates within the system).

A system that is built on an open architecture is generally more flexible in the kinds of applications that it can accommodate, and thus can benefit from availability of third-party components that are also built on an open architecture.

A system that is built on a closed architecture is generally simpler to design and implement because you can use the prior knowledge of the system when you design each device's interface and behavior.

Because the functionality of a Pyxos FT Pilot is most likely tied to the application for which it is designed, a Pilot's architecture is likely to be a closed one. A Pilot needs to know the kinds of Points that are part of the Pyxos FT network so that it can register them and interact with them. A Pilot also needs to know how the system uses the data that it processes for the Points.

A Pyxos FT Point, however, can provide general functions for an application or very specific ones. Thus, a Point's architecture can be either open or closed, depending on your design goals. If your Point will be used in multi-vendor environments, for example, with a Pyxos FT Pilot that you do not design, then a more open architecture is appropriate. However, if your Point will be used only in networks over which you have design control, a more closed architecture might be appropriate.

Additionally, system interoperability can affect whether a system's design is more open or more closed. See *System Interoperability* on page 10 or the *Pyxos FT Programmer's Guide* for more information.

System Architecture: Static or Dynamic

In addition to being open or closed, the architecture for a Pyxos FT system can be basically static or basically dynamic. A static architecture is one that has a fixed number of devices and the interaction between the devices is well defined. A dynamic architecture is one that has a varying number of devices of particular type and varying interactions between the devices. In general, a system's architecture is not completely static or completely dynamic, but lies somewhere between the extremes.

A static system is generally easier for a user to set up, and often requires no user interaction at all (for example, by using hardwired registration for a Pyxos FT Point). However, a static system can be difficult to expand if additional functionality is required. A static system can also be more difficult to integrate with devices from multiple vendors.

A dynamic system generally provides greater variety in the kinds of configurations that it can support, but often requires some user interaction during the installation and registration process. For example, a dynamic system that has separate Points for light switches and for lamps would require user interaction to register a particular switch to control a particular

lamp because the system has no prior knowledge of which switch should be paired with which lamp. However, the variety of supported configurations often allows a system to be more easily integrated with devices from multiple vendors.

For a Pyxos FT Point, the registration method that it uses affects how static or dynamic its design is:

- Hardwired registration
    - No user interaction required
    - Identifying each instance of a device requires some external identifier, such as a wiring harness
    - More difficult to use hardwired Points in multiple systems, that is, the architecture is fairly closed
- Automatic registration
    - No user interaction required
    - Somewhat difficult to distinguish between each instance of a device
- Manual registration
    - User interaction required, for example, to press a Join button
    - User is responsible for identifying different instances of a device

System Maintenance

System design affects how a device can be maintained in the field. General considerations, such as the placement of a Service pin or Join button within a device enclosure, are common to many devices. For a Pyxos FT network, there are other considerations, some of which are described in *Hardware Design Considerations* on page 11. In addition to hardware considerations, one of the other significant considerations involves removal and replacement of Pyxos FT Points within an active network.

The primary design consideration for removal and replacement of Points is whether the removal or replacement should be automatic (handled by the Pilot) or under user control.

When a Point experiences a persistent failure (either of the device or of its communication with the network), the Pilot can decide to remove the failed or non-responsive Point from the network. Such automatic removal can interfere with automatic recovery if that Point is later reconnected to the network, and can also lose user-defined data. However, removal of a failed or non-responsive Point frees its timeslot so that another device can join the network. User-initiated removal can be appropriate for relatively static systems, and is generally required to add new devices to the network.

There are times when a user wants to replace one Point with another of the same type (the same program interface). For automatic replacement, the Pilot must be able to distinguish between replacing an existing Point and adding a new Point to the network, which generally depends on how dynamic the system is. User-initiated replacement is required for plug-press-and-play installations and for unhosted Points.

System Interoperability

Designing a system for interoperability is largely dependent on firmware-design considerations, but also can depend on hardware design that affects data encoding. For

example, the Pilot must be able to understand the format of the data from every Point in the network, which includes the byte order of the data and how the data is packed.

If the Pyxos FT network is connected to an external network, such as a LONWORKS network, the Pilot must be able to interact with the network management tools for that network, such as the LonMaker® Integration Tool, and provide supervisory control of both the Pyxos FT network and its part of the external network.

Pyxos FT networks can use the same data type definitions that are defined by LonMark® and Echelon for LONWORKS networks. These network variables not only represent a wide variety of data types that are used in control systems, but they also allow for seamless integration between Pyxos FT networks and LONWORKS networks.

Manufacturers of Pyxos FT devices can provide standard interface descriptions of their devices for other manufacturers to use during design of their devices. The interoperable device interface can be similar to the external interface file (.XIF) that LONWORKS networks use.

Hardware Design Considerations

Hardware design for Pyxos FT devices primarily involves design considerations for the following areas of the system:

- Power distribution and Electromagnetic Compatibility (EMC)
- Communications, including topology choices
- Node design, including Point type and host microprocessor choices

In addition, your hardware design must include such general considerations as:

- Design for reliability, which can include decisions about battery backup for the Pilot or critical Points, short-circuit protection within a device, and so on.
- Device size and packaging, which can influence other decisions
- Cost of manufacturing and pricing for the final product, both of which can influence other decisions

This section addresses hardware considerations that are specific to Pyxos FT systems. The more general considerations are also important, but are beyond the scope of this manual.

Power Considerations

For the design of a Pyxos FT network, the primary power considerations include:

- Whether the device uses link power or local power
- Whether the device uses AC or DC link power
- What kind of filtering or conditioning the power source needs
- Whether the Pilot sends data continuously or only on-demand
- Design considerations for EMC, including immunity from environmental and noise effects

For link-powered systems, you need to include proper isolation for each node's power supply. The isolation circuits are simple inductor-capacitor (LC) circuits that:

- Provide high impedance at data communication frequencies to prevent network disturbance

- Allow the low frequency power (DC or 50-60 Hz AC) to flow into the devices

For more information about these isolation circuits, see *Source Power Supply* on page 55 and *Node Power Supply for Link Power* on page 57.

Each Pyxos FT device requires 3.3 VDC power. A Pyxos FT device can receive power in one of two ways, from a local power supply or from the Pyxos FT network cable. A device that receives power over the Pyxos FT network cable is receiving *link power*. For a locally powered device, you can use any power supply that meets your application's requirements. For a link-powered device, the power supply must be either 24 VAC (50–60 Hz) or 24 VDC. For more information about link power, see Chapter 6, *Link Power*, on page 53.

A Pilot can send network data continuously or on-demand. When a Pilot or Point sends data on-demand, it consumes transmit power only while it is actively sending the data, thus devices in an on-demand system can conserve power, for example, for a battery-based power supply. Using link power, each Point in the network can also receive data on-demand. In this case, you should design your source power supply to handle all of the Points' concurrent demand for power. Such systems are best suited to networks that require few or infrequent updates. See the *Pyxos FT Programmer's Guide* for more information about designing on-demand networks.

You should design your Pyxos FT devices for EMC, so that they are able to pass various rigorous tests for immunity to external interference and to demonstrate low electromagnetic interference (EMI) emissions. If the product will be sold in the European Union (EU), the product must demonstrate immunity to certain external influences to pass European Conformité Européene[3] (CE) Marking tests. Even if the product will not be sold in the EU, such immunity testing helps you to design a better, more robust product. Echelon has performed immunity tests for CE Marking on Pyxos FT devices, and has also performed additional tests to ensure immunity and low EMI. However, you need to perform your own immunity testing for Pyxos FT devices that you design and build. For more information about EMC, see Chapter 7, *Design and Test for Electromagnetic Compatibility*, on page 63.

Communications Considerations

For the design of a Pyxos FT network, the primary communications considerations include:

- What topology your network expects or can tolerate
- What wire gauge your network requires
- Which coupling circuit the network connection uses
- What response times are expected for minimum and maximum configurations
- How much distance you allow from one Point to another and from any Point to the Pilot

The network topology that your Pyxos FT network uses affects how the network cable must be terminated. For a free-topology network, the cable needs a single terminator anywhere on the network. For a bus-topology network, the cable needs to be doubly terminated, one terminator at each end of the bus. Having incorrect termination for the network can negatively affect network communication reliability. For more information about network termination, see *Network Termination* on page 49.

If you use link power for your Pyxos FT network, the type of wire that you use affects the maximum length allowed from the power source to the device. In general, a larger gauge

[3] European Conformity

wire can carry more current, and thus provides more distance. For more information about how wire size affects link power distance limitations, see *Distance Limitations for Link Power* on page 58; for information about cable selection, see *Network Cabling* on page 48.

Each Pyxos FT device can connect directly to the Pyxos FT network or can couple to the Pyxos FT network through a coupling circuit. The coupling circuit helps provide isolation for the device when the device's ground differs from the network's. How the device couples to the network can also affect its Electromagnetic Compatibility (EMC). A Pyxos FT device can use one of four different topologies for the coupling circuits:

- Direct-connect
- Non-isolated
- Floating
- Transformer-isolated

For more information about these coupling circuits, see *Network Coupling Circuits* on page 37.

Network response time for a Pyxos FT network depends mostly on the number of timeslots that are defined for the system. A system that has few timeslots (for example, 4) has a faster network response time than a system that has the maximum number of timeslots (32) defined. When you design your Pyxos FT Point or system, you might not know how many timeslots will be defined for the network, so you should allow your devices to handle a minimum response time. For more information about timeslot allocation, see the *Pyxos FT Programmer's Guide*.

The allowable distance from one Point to another and the allowable distance from a Point to the Pilot are determined primarily by the network cable choice and the network topology used. For a network that uses link power, the choice of network cable and of network topology directly determines the allowable distances. For locally powered networks, the primary determinant is the network topology.

Node Design Considerations

For the design of a Pyxos FT network, the primary node design considerations include:

- Whether the node is a Pilot or a Point
- For Points: Whether it is a hosted or unhosted Point
- For hosted Points: Which registration method should the Point use (unhosted Points use manual registration)
- For hosted Points and for a Pilot: What host microprocessor does it require, which can be influenced by the Serial Peripheral Interface (SPI) requirements of the device
- For the host microprocessor: What development environment meets your requirements
- Whether the Pilot requires connectivity to outside networks, such as LONWORKS networks
- How many Points the network can include, which determines how many timeslots are required for the network

Whether a Pyxos FT device is a Pilot or a Point is determined by the needs of your application. For both Pilots and Points, you should consider addressing the architectural design decisions described in *System Design Considerations* on page 8. A Pilot acts as the

coordinator for all activities in the network, and thus is generally a more sophisticated device than a Point. Most Pyxos FT Points are simple devices that perform a few functions for local I/O and report status to the Pilot; however, you can design as sophisticated a Point as your application requires.

If you are designing a Pyxos FT Point, one of the first decisions that you need to make is whether the Point requires a host microprocessor. An unhosted Point can manage up to four bidirectional digital I/O functions and one additional input-only digital I/O function. A hosted Point can manage as many digital or analog I/O functions as its host microprocessor (and associated peripherals) can support. In general, an unhosted Point is smaller, consumes less power, and is less expensive to manufacture than a hosted Point.

Related to the decision about whether the Point is hosted or unhosted, you need to decide what registration method the Point uses. For unhosted Points, the only choice is manual registration, which means that a user must interact with the device during registration (such as pressing a Join button). For hosted Points, you have three choices: automatic, manual, and hardwired registration. For automatic registration, you might have no associated hardware design constraints, but for manual and hardwired registration, you need to include an interface for the registration mechanism, such as a button or a connection to a wiring harness.

For hosted Points and for a Pilot, you need to decide what microprocessor to use as the host. In general, you can use any microprocessor that meets your application needs. However, you need to ensure that the microprocessor has sufficient RAM and program memory to accommodate the Pyxos FT API, if you use it. See *Selecting a Host Microprocessor* on page 26 for more information about what to consider when selecting a host microprocessor. Your choice can also depend on the SPI requirements of your device, such as communication performance and available bandwidth.

A hosted Point or a Pilot runs a firmware application program to provide the needed functions of the device. After you select the host microprocessor, you need to choose a hardware and firmware development environment, including prototyping boards, compilers and assemblers, code project management systems, in-circuit emulators, and so on. Chapter 7 of the *Pyxos FT EVK User's Guide* provides suggestions for development environments for the host microprocessors that the Pyxos FT EVK uses: the Atmel® ARM® AT91SAM7S64 microprocessor (an ARM7-family microprocessor) and the Atmel AVR® ATtiny13 microprocessor.

One of the design decisions that impacts both the hardware and firmware design of the Pilot is whether your system requires connectivity to another network, such as a LONWORKS network. A connection to a LONWORKS network requires an additional network connector, a Neuron Chip or Echelon Smart Transceiver, and associated communications hardware. It also requires that your firmware application program use the LonTalk® protocol to communicate with the network. Other external network types have similar requirements.

Finally, your design should accommodate the network communications requirements discussed in *Communications Considerations* on page 12, such as how many Points your network allows.

Firmware Design Considerations

For a Pyxos FT Pilot and for hosted Pyxos FT Points, you need to consider the firmware design while designing the device. Firmware design is affected primarily by the choice of host microprocessor for the device because each microprocessor has different amounts of RAM and program memory available for the firmware and for the data that the firmware processes.

Along with the choice of firmware development environment, you need to decide whether the firmware application programs will use the Pyxos FT API. A Pyxos FT Pilot should almost always use the Pyxos FT Pilot API, but some Pyxos FT Points might be designed with host microprocessors that have too little program memory to accommodate the Pyxos FT Point API. For Points that do not use the Pyxos FT Point API, the firmware application program communicates directly with the Pyxos FT Chip using the host microprocessor's SPI interface.

For more information about firmware design, including the Pyxos FT protocol and the Pyxos FT API, see the *Pyxos FT Programmer's Guide*.

3

Pyxos FT Hardware Resources

This chapter provides an overview of the hardware resources for the Pyxos FT Chip, including operating parameters and chip pinouts.

Overview

The Pyxos FT Chip provides a twisted-pair free topology transceiver along with the Pyxos FT protocol engine on a single chip. You can connect the Pyxos FT Chip to a host microprocessor (in this case, the chip runs in hosted mode) or you can operate it standalone (in this case, the chip runs in unhosted mode).

The main components of the Pyxos FT Chip, as shown in **Figure 1**, include:

- SPI port and digital I/O – serial peripheral interface (SPI) for communicating with external I/O devices
- Control registers – registers for interacting with the Pyxos FT protocol and for controlling the Pyxos FT Chip
- Index and timeslot memory – 1 KB static random access memory for temporary storage of Pyxos Chip Index (PCI) and timeslot information
- Protocol engine – the main processing engine for the Pyxos FT Chip
- Clock and reset – on-chip clock and power-on-reset functions
- XCVR – transceiver for the Pyxos FT network

The pinout labels shown in **Figure 1** are described in *Pyxos FT Chip Pin Assignments* on page 20.

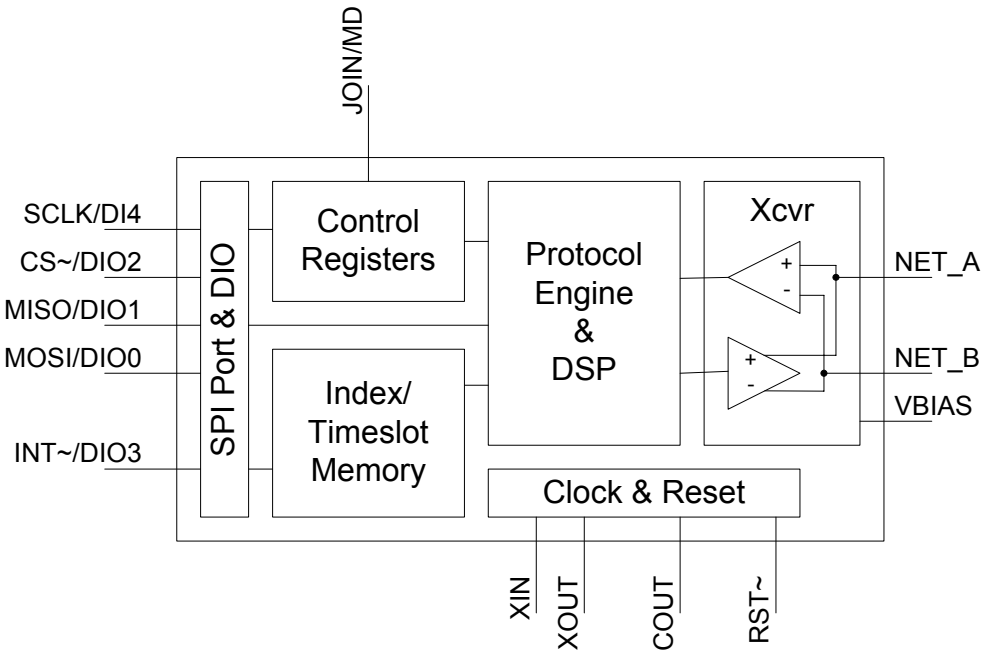

Figure 1. Pyxos FT Chip Block Diagram

When the Pyxos FT Chip runs in hosted mode, a host microprocessor communicates with the Pyxos FT Chip through the SPI port. When the Pyxos FT Chip runs in unhosted mode, the SPI pins become general purpose digital inputs or outputs.

The control registers, timeslot memory, and Pyxos Chip Index (PCI) memory share the same address space and are accessible from either the SPI or the Pyxos FT network. The control

registers configure the Pyxos FT Chip, and send and receive control data over the network. The timeslot memory contains data items that are sent and received over the network by a Pyxos FT Pilot. The PCI memory contains data items that are sent or received over the network by Pyxos FT Points.

The protocol engine interprets commands received from the control registers to transfer data over the network.

The transceiver block processes and interprets the signals on the network to send and receive network data.

For more information about the Pyxos FT Chip registers and the Pyxos FT protocol, see the *Pyxos FT Programmer's Guide*.

Operating Range

Table 2 describes the standard operating conditions for the Pyxos FT Chip.

Table 2. Pyxos FT Chip Operating Conditions

Parameter[1]	Description	Minimum	Typical	Maximum
V_{DD3}	Supply voltage	2.97 V	3.3 V	3.63 V
T_A	Ambient temperature	-40 ºC		+85 ºC
f_{xin}	Clock frequency	9.9975 MHz	10.0000 MHz	10.0025 MHz
I_{DD3-RX}	Current consumption in receive mode[2]		7 mA	10 mA
I_{DD3-TX}	Current consumption in transmit mode[2]		25 mA	30 mA

Notes:

1. All parameters assume nominal supply voltage (V_{DD3} = 3.3 V ± 10%) and operating temperature (T_A between -40 ºC and +85 ºC), unless otherwise noted.
2. Assumes no load on digital I/O and 50 Ω across the NET_A/NET_B pins.

A Pyxos FT Pilot is in transmit mode approximately 50% of the time that it operates. A Pyxos FT Point is in transmit mode only during its read timeslot, thus a Point transmits data approximately 1/(2N) of the time that it operates, where N is the number of timeslots defined for the Pyxos FT network. Thus, the numbers in **Table 2** for current consumption in transmit mode represent peak values rather than continuous usage values.

Table 3 on page 20 describes the absolute maximum conditions for the Pyxos FT Chip. Absolute maximum ratings are limits beyond which the device might become damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Table 3. Pyxos FT Chip Absolute Maximum Ratings

Parameter	Description	Minimum	Maximum
V_{DD3}	Supply voltage	-0.3 V	+3.7 V
$V_{i\text{-}digitalIn}$	Input voltage – digital input pins	-0.3 V	+5.5 V
$V_{i\text{-}other}$	Input voltage – other non-power pins	-0.3 V	V_{DD3} + 0.3 V
I_i	Input current – all non-power pins	-10 mA	+10 mA
$T_{storage}$	Storage temperature	-55 ºC	+125 ºC

Pyxos FT Chip Pin Assignments

Figure 2 shows the pinout for the Pyxos FT Chip. The figure does not show the bottom pad (pin 21).

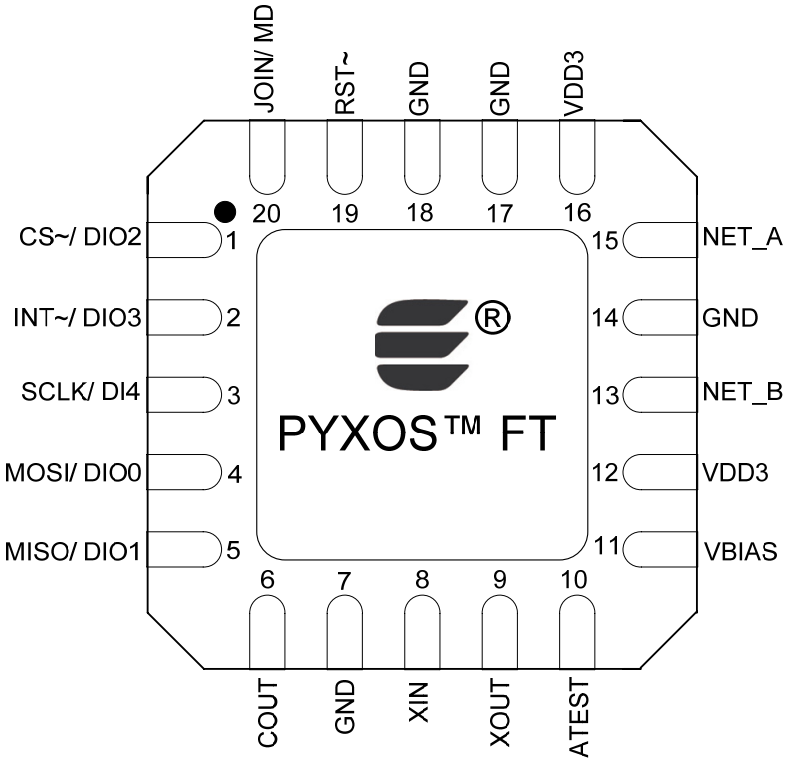

Figure 2. Pyxos FT Chip Pinout Diagram

Table 4 on page 21 lists the pin assignments for the Pyxos FT Chip. The name and description for pins 1 to 5 on the Pyxos FT Chip vary depending on whether the chip is used for a Pilot or hosted Point or is used for an unhosted Point. All of the other pins have the same functionality for both unhosted Points and for hosted Points and Pilots.

All digital inputs are low-voltage transistor-transistor logic (LVTTL) compatible, low leakage, 5 V tolerant, with hysteresis. All digital outputs are slew-rate limited to reduce Electromagnetic Interference (EMI) concerns

Table 4. Pyxos FT Chip Pin Assignments

Name	Pin Number	Type	Description	
			Hosted	Unhosted
CS~ / DIO2	1	Digital I/O	SPI Slave Select Input (Active low)	General Purpose Digital I/O
INT~ / DIO3	2	Digital I/O	Interrupt Output (Active low)	General Purpose Digital I/O
SCLK / DI4	3	Digital In	SPI Clock Input	General Purpose Digital Input
MOSI / DIO0	4	Digital I/O	SPI Slave Input	General Purpose Digital I/O
MISO / DIO1	5	Digital I/O	SPI Slave Output	General Purpose Digital I/O
COUT	6	Digital Out	Clock Output	
GND	7	Ground	Ground	
XIN	8	Oscillator In	Crystal Oscillator Input	
XOUT	9	Oscillator Out	Crystal Oscillator Output	
ATEST	10	Analog I/O	Analog Test (Can connect to ground or leave floating)	
VBIAS	11	Analog Out	Transceiver Common-Mode Bias Voltage Output	
VDD3	12	Power	3.3 V Power	
NET_B	13	Analog I/O	Network Port (Polarity Insensitive)	
GND	14	Ground	Ground	
NET_A	15	Analog I/O	Network Port (Polarity Insensitive)	
VDD3	16	Power	3.3 V Power	
GND	17	Ground	Ground	
GND	18	Ground	Ground	

Name	Pin Number	Type	Description	
			Hosted	Unhosted
RST~	19	Digital I/O	Reset I/O (Active low)	
JOIN / MD	20	Digital In	Join and Mode Select	
Pad	21	Do Not Connect	Do Not Connect	

Characteristics of the Digital I/O Pins

Table 5 lists the characteristics of the digital I/O pins. All pins can withstand 2 kV Electrostatic Discharge (ESD) voltage, as tested according to MIL-STD-883 Method 3015.7.

In addition, the NET_A, NET_B, and VBIAS pins can withstand 8 kV ESD voltage, as tested according to the Human Body Model, MIL-STD-883 Method 3015.7 and ESD Association standard ESD STM5.1.

Table 5. Pyxos FT Chip Digital Pin Characteristics

Parameter[1]	Description	Minimum	Maximum
V_{oh}	Output drive high at I_{oh} = –8 mA	V_{DD3} – 0.6 V	V_{DD3}
V_{ol}	Output drive low at I_{ol} = 8 mA	0 V	0.5 V
V_{ih}	Input high level	2.1 V	5.5 V
V_{il}	Input low level	0 V	0.7 V
V_{hys}	Input hysteresis	400 mV	
I_{pu}	Input pullup current[2] at V_i = 0 V	–30 µA	–200 µA
t_{slr}	Slew-rate limited rise time[3]	1.2 ns	10 ns
t_{slf}	Slew-rate limited fall time[3]	1.2 ns	10 ns

Notes:

1. All parameters assume nominal supply voltage (V_{DD3} = 3.3 V ± 10%) and operating temperature (T_A between -40 ºC and +85 ºC), unless otherwise noted.
2. Applies to Reset (RST~) pin only.
3. Slew rate rise and fall times are measured between the 10% and 90% points on the waveform with 1.5 pF load capacitance.

The Reset Pin

The Reset (RST~) pin is bidirectional:

- When the Pyxos FT Chip performs an internal reset, it asserts the RST~ pin.
- When an external device asserts the RST~ pin, the Pyxos FT Chip resets.

The Pyxos FT Chip includes an on-chip low-voltage interrupt (LVI) that asserts the RST~ pin when V_{DD3} falls below the LVI threshold voltage. **Table 6** summarizes the reset parameters.

Table 6. Reset Pin Parameters

Parameter[0]	Description	Minimum	Typical	Maximum
V_T	LVI threshold voltage	2.7 V		2.95 V
t_{R-IN}	Reset pulse width required to reset the Pyxos FT Chip	250 ns		
t_{R-OUT}	Reset output pulse width		412.5 µs	

Note:

All parameters assume nominal supply voltage (V_{DD3} = 3.3 V ± 10%) and operating temperature (T_A between -40 ºC and +85 ºC), unless otherwise noted.

Important: Do not drive the RST~ pin high. You can connect a high impedance device (that is, an input) or an open-collector or open-drain output to this pin. In either of these cases, you generally do not need to include an external pullup resistor to your circuit because the Pyxos FT Chip includes an internal pullup resistor for the RST~ pin.

The Pyxos FT Chip can also be reset over the network or from the SPI port. If you write the values 0xDE 0xAD 0xBE 0xEF to Pyxos Chip Index (PCI) 0xFA (SPI addresses 0x3E8 to 0x3EB), the Pyxos FT Chip performs an internal reset and pulses the RST~ output pin low.

The Join and Mode Select Pin

The Join and Mode Select (JOIN/MD) pin serves two functions:

- It determines whether the Pyxos FT Chip runs in hosted mode (connected to a host microprocessor) or in unhosted mode.
- It triggers a registration request message as part of manual registration for a Point.

The Pyxos FT Chip samples this pin during reset to determine whether the chip should operate in hosted mode or unhosted mode:

- If the pin is low during reset, the Pyxos FT Chip operates in hosted mode, and enables the SPI port.
- If the pin is high during reset, the Pyxos FT Chip operates in unhosted mode, and enables the DIO interface.

See *Specifying Hosted or Unhosted Operating Mode* on page 26 for more information about how the Join and Mode Select pin determines the Pyxos FT Chip's operating mode.

Pyxos FT Chip Clock

The Pyxos FT Chip requires a 10 MHz oscillator, with a frequency accuracy of ± 250 ppm over the full range of component tolerances, operating conditions, and crystal aging. Variations within the Pyxos FT Chip use up a portion of the overall ± 250 ppm budget, and the remaining portion of the error budget allocated for total crystal uncertainty is ± 135 ppm. Total crystal uncertainty is the combination of the crystal's initial frequency tolerance plus its temperature and aging tolerances.

The Pyxos FT Chip has been designed to work with an 18 pF parallel resonant crystal, such as the Abracon CMR309T10.000MABJTR in the HC49US surface mount package. The crystal is required; the Pyxos FT Chip's XIN pin should not be driven from an external source.

The 3.3 V COUT clock output signal provides a buffered version of the clock signal that you can use for other circuitry that requires a 10 MHz clock (such as a host microcontroller). If the chip's COUT clock output is routed to another device on the printed circuit board, you should place a 49.9 Ω "back termination" resistor directly adjacent to the Pyxos FT Chip, in series with that connection to reduce ringing.

For more information, see *Design Considerations for the Pyxos FT Chip Clock* on page 33.

SPI Slave Mode Port (Hosted Mode)

The Pyxos FT Chip includes a Serial Peripheral Interface (SPI) Slave Mode interface to allow host microprocessors to configure the chip and communicate with other devices on the network. This SPI port is available only when the Pyxos FT Chip runs in hosted mode.

The SPI interface consists of the standard 4-pin SPI slave mode interface (CS~, SCLK, MOSI, and MISO) plus an interrupt signal (INT~). A host microprocessor can interface to the Pyxos FT Chip by using as few as two pins (using the SCLK pin and tying the MOSI and MISO pins together). Higher performance microprocessors can use all five pins to take advantage of the interrupt and other features.

See chapter 6 of the *Pyxos FT Programmer's Guide* for more information about the Pyxos FT SPI.

4

Pyxos FT Node Design

This chapter describes design considerations for Pyxos FT nodes, including designs for unhosted and hosted nodes, microprocessor considerations, coupling circuits, and layout guidelines.

Overview

A Pyxos FT device can be as simple as an unhosted Point (which requires only the Pyxos FT Chip, a power supply, and associated digital I/O) or as sophisticated as a Pyxos FT Pilot (with a high performance microprocessor, power supply, local I/O, and a LONWORKS connection). The Pyxos FT Chip is designed to work easily in both simple and sophisticated designs. This chapter describes node design so that you can effectively use the many features of the Pyxos FT Chip.

Figure 3 shows a generic block diagram of a Pyxos FT Pilot or hosted Pyxos FT Point. The host microprocessor communicates with the Pyxos FT Chip through the SPI port, and could also include local I/O, and (for a Pilot) a connection to a LONWORKS channel. The network coupling circuit provides electrical isolation between the network and Pilot or Point. The Join/Mode button controls whether the Pyxos FT Chip is operating in hosted or unhosted mode, and is used for manual Point registration. Power can be distributed over the network (link power) or can be available locally.

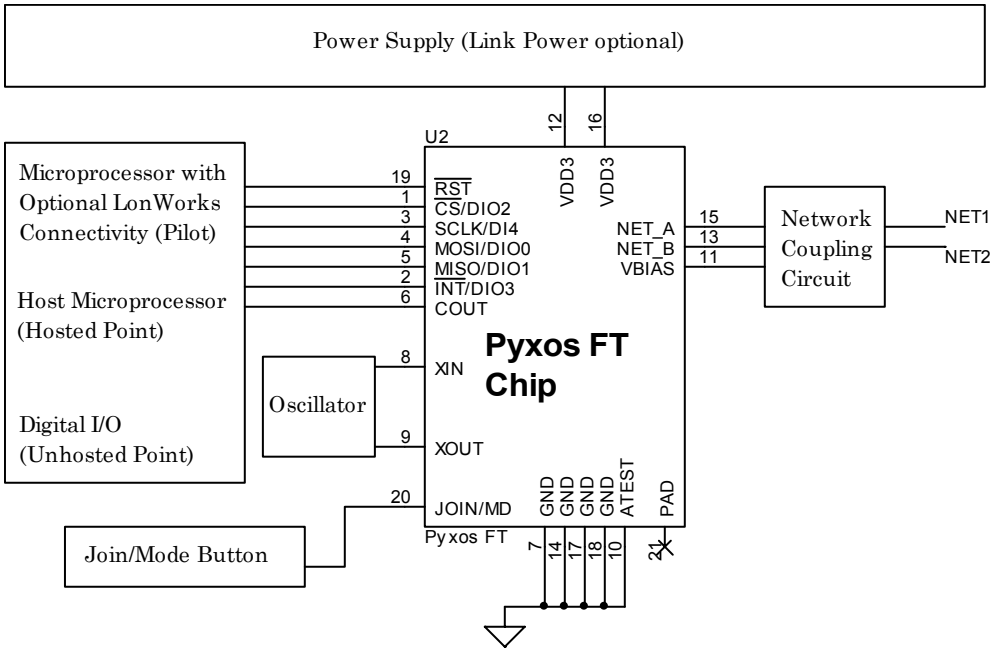

Figure 3. Generic Pyxos FT Pilot or Hosted Pyxos FT Point

The rest of this chapter provides more detail about the circuitry used with a Pyxos FT Chip and the options available. Information about link power design is in Chapter 6, *Link Power*, on page 53, and information about network system design is in Chapter 2, *Pyxos FT System Design Principles*, on page 7.

Specifying Hosted or Unhosted Operating Mode

The Pyxos FT Chip can operate with or without a host microprocessor. A Pilot always has a host microprocessor, but a Point can be either hosted or unhosted. When the Pyxos FT Chip is hosted, the host microprocessor has access to the chip's SPI port (pins 1 to 5); when the Pyxos FT Chip is unhosted, your application has access to the chip's digital I/O (also pins 1 to 5). To specify whether the Pyxos FT Chip is hosted or unhosted, you need to include a simple resistor-capacitor (RC) circuit on the Join and Mode Select (JOIN/MD) pin (pin 20).

Figure 4 shows the circuitry required to specify hosted mode for the Pyxos FT Chip. A hosted Point can use any of the registration methods (automatic, hardwired, or manual), so the figure shows two allowable circuits:

- For manual registration, a switch is required to force a transition on the JOIN/MD pin to trigger a registration request.
- For automatic or hardwired registration, you can simply connect the JOIN/MD pin to ground.
- For a Pilot, you can simply connect the JOIN/MD pin to ground.

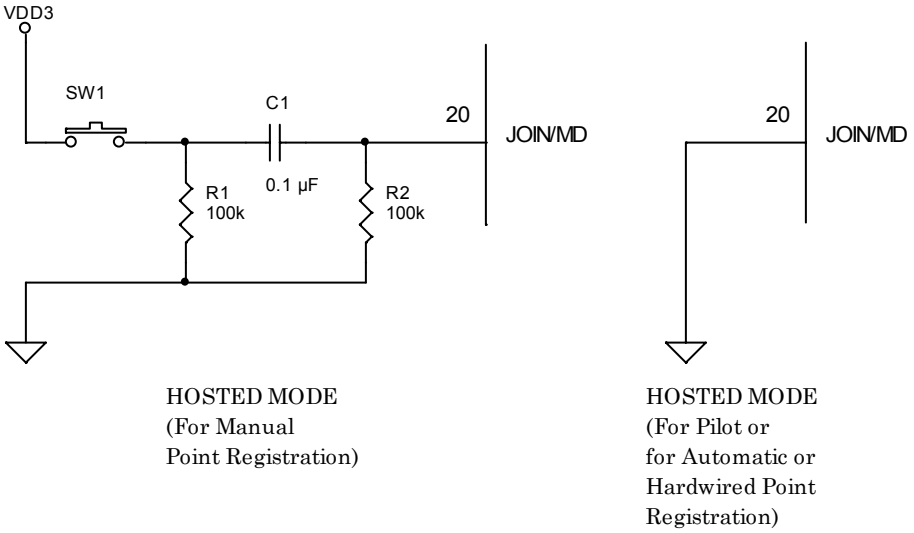

Figure 4. Circuitry to Specify Hosted Mode

Figure 5 shows the circuitry required to specify unhosted mode for the Pyxos FT Chip. An unhosted Point must use manual registration, thus the circuit includes a switch.

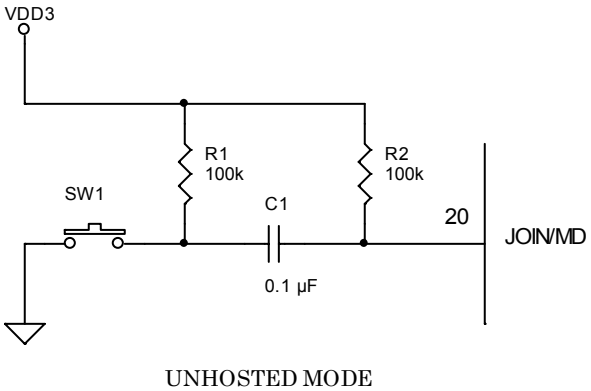

Figure 5. Circuitry to Specify Unhosted Mode

A transition on the JOIN/MD pin from the normal state to the opposite state during normal operation initiates a registration request. For a hosted Pyxos FT Point, this transition is the rising edge; for an unhosted Pyxos FT Point, this transition is the falling edge. Registration request messages are used only for manual registration; hardwired and automatic registration do not use this pin.

A free timeslot request message can be sent only in response to a free timeslot advertisement by the Pilot, and this message goes out only on one of the timeslots that is advertised as free.

After the registration request message is successfully delivered, the message is not re-sent until the Pyxos FT Chip detects another active-edge transition on the JOIN/MD pin.

Unhosted Points

For a Pyxos FT Chip in unhosted mode, you have access to five general-purpose digital I/O pins (four bidirectional input and output, plus one input only):

- Digital I/O 0 (DIO0)
- Digital I/O 1 (DIO1)
- Digital I/O 2 (DIO2)
- Digital I/O 3 (DIO3)
- Digital Input 4 (DI4)

You can connect these I/O pins to any 3V-compatible digital I/O, such as switches, LEDs, or I/O for devices.

When the Pyxos FT Chip resets (that is, when the RST~ pin is asserted), all of the digital I/O pins have high impedance until they are configured.

For the digital I/O pins, you should ensure that the rate at which the inputs toggle does not exceed the frame rate of the Pyxos FT network. The Pyxos FT Chip samples the inputs as the data packet is being assembled, thus if, for example, two transitions occur on an input pin prior to sampling, then information can be lost.

In addition, if you set the I/O mode for the unhosted Point to Send Updates On Change (rather than Polled) in the Point's properties (defined in the Pyxos FT Interface Developer utility), any input transition on the digital I/O pins causes the Point to enqueue an I/O message to the Pyxos FT network. Thus, you should ensure that the aggregate change rate (that is, the change on any input pin) is limited to ≤ 5 MHz to prevent overwhelming the internal resources of the Pyxos FT Chip.

Figure 6 on page 29 shows the relevant pin connections for a Pyxos FT Chip in unhosted mode. The pin connections for the five digital I/O pins are not fully specified because these connections depend on your application.

Recommendation: For any of the digital I/O pins that your application does not use, connect the unused pin either to V_{DD3} or to ground. This connection can also include an optional 10 kΩ resistor.

As described in *Specifying Hosted or Unhosted Operating Mode* on page 26, the JOIN/MD pin must be set high during chip reset to specify unhosted mode for the Pyxos FT Chip. **Figure 6** also shows the connection for the Reset pin. Other pin connections are not shown.

The figure shows a switch connected to the Join and Mode Select (JOIN/MD) pin because an unhosted Point must use manual registration.

The two capacitors (C2 and C3) shown connected to the RST~ pin might not be necessary for most Point designs, depending on the device's electrostatic discharge (ESD) performance. See *Design and Test for Electromagnetic Compatibility* on page 63 for information about ESD testing of devices.

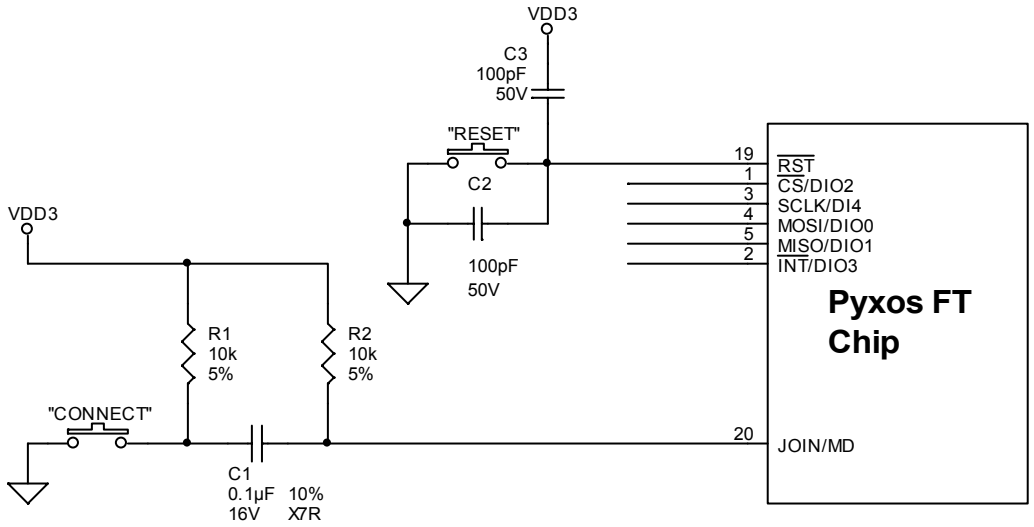

Figure 6. Pin Connections for a Pyxos FT Chip in Unhosted Mode

Pilot and Hosted Points

For a Pyxos FT Chip in hosted mode you have access to a standard 4-pin SPI slave mode interface, which includes the following signals:

- Chip select (CS~)
- SPI clock input (SCLK)
- Master-out slave-in (MOSI)
- Master-in slave-out (MISO)

The interface also includes an interrupt signal (INT~) that can be used to improve host microprocessor response times.

Figure 7 on page 30 shows the relevant pin connections for a Pyxos FT Chip in hosted mode, where the host is an ARM7-family microprocessor, the Atmel ARM AT91SAM7S64. Because the ARM7 microprocessor has a hardware SPI port, the ARM7 microprocessor's interface to the Pyxos FT Chip uses all five pins to take advantage of the chip select (CS~) to address the Pyxos FT Chip and frame data transfers, the interrupt (INT~) to coordinate network activity, the SPI transfer clock (SCLK), and the serial data I/O lines (MOSI and MISO).

Figure 8 on page 31 shows the relevant pin connections for a Pyxos FT Chip in hosted mode, where the host is an AVR microprocessor, the Atmel AVR ATtiny13. Because the AVR microprocessor does not have a hardware SPI port, the AVR microprocessor's interface to the Pyxos FT Chip uses just two pins: the SPI transfer clock (SCLK) and the serial data I/O lines (MOSI and MISO) tied together. The ATtiny13 does not use the chip select (CS~) or the interrupt (INT~) pins. A firmware program for the ATtiny13 manages the communication with the Pyxos FT Chip directly by using a software bit-bang technique.

Refer to the documentation for your host microprocessor for information about how to use the host's SPI master port, and refer to the *Pyxos FT Programmer's Guide* for information about the Pyxos FT Chip's SPI slave port.

As described in *Specifying Hosted or Unhosted Operating Mode* on page 26, the JOIN/MD pin must be set low during chip reset to specify hosted mode for the Pyxos FT Chip. Both figures also show the connections for the Pyxos FT Chip Reset pin (RST~) to the host

microprocessor Reset pin (NRST~ for the ARM7 and RESET~ for the AVR). Other pin connections are not shown.

The figures show a switch connected to the Join and Mode Select (JOIN/MD) pin, but if the node is a Pilot or a hosted Point that uses automatic or hardwired registration, the switch is not required.

The two capacitors (C1 and C2) shown connected to the RST~ pin might not be necessary for most Pilot or Point designs, depending on the device's ESD performance. See Chapter 7, *Design and Test for Electromagnetic Compatibility*, on page 63 for information about ESD testing of devices.

The 49.9 Ω resistor (R1) that is connected to the ARM7 SPCK pin and to the AVR (ATtiny13) PCINT0 pin is a back-termination resistor that helps reduce ringing of the signal on the Pyxos FT Chip's SCLK pin. Place this resistor on the PCB so that it is physically near the host microprocessor.

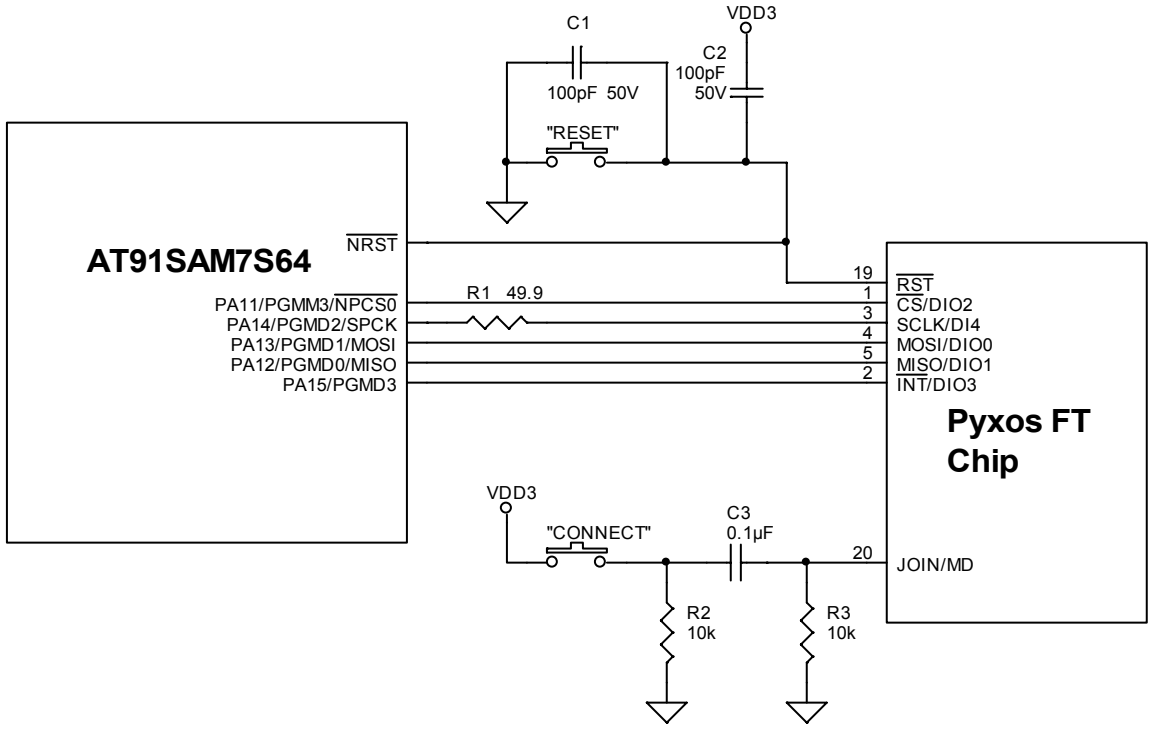

Figure 7. Pin Connections for a Pyxos FT Chip in Hosted Mode (ARM7 Host)

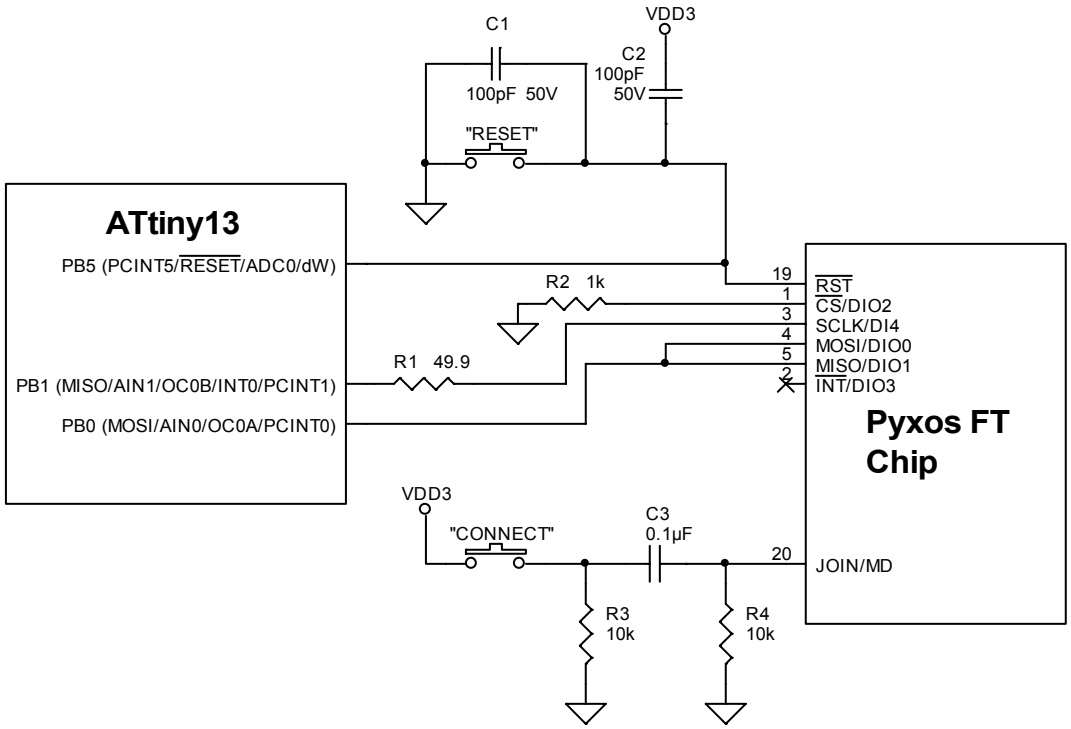

Figure 8. Pin Connections for a Pyxos Chip in Hosted Mode (AVR Host)

Selecting a Host Microprocessor

You can use the Pyxos FT Chip with any of a wide variety of host microprocessors. Thus, your choice of host microprocessor is influenced only by the design requirements of your Pyxos FT device, including such considerations as cost, performance, power consumption, size, embedded peripherals, and development tools. For example, the Pyxos FT EVK Evaluation Kit includes an example design that uses a low-end, inexpensive microprocessor that has limited hardware resources (the Atmel AVR ATtiny13 microprocessor), and another example design that uses a high-performance microprocessor with hardware SPI and ANSI C support (the Atmel ARM AT91SAM7S64 microprocessor).

When selecting a host microprocessor to work with the Pyxos FT Chip, you should consider the following factors:

- Compute performance:
    - A Pilot generally needs greater compute performance than a Point because the Pilot manages the network traffic flow between Points and with external devices or networks. The performance requirements scale with the number of Pyxos Network Variables (PNVs) that are defined for the system, and depend on the kinds of computations that your application needs to perform on the data.
    - A Point generally needs much less compute performance than a Pilot. The performance requirements for a Point depend mainly on the I/O requirements of the Point.

- Program memory:
    - The host microprocessor must have enough nonvolatile program memory to store the firmware application programs for your Pilot or Point applications.
    - A Pilot uses the Pyxos FT Pilot application programming interface (API). This API requires approximately 5 to 6 KB of host microprocessor program memory, depending on what features your application uses, plus approximately 0.5 KB for the Pyxos FT Serial API.
    - A hosted Point can use the Pyxos FT Point API or not, depending on the available program memory of the host microprocessor. This API requires from approximately 0.6 to 1.5 KB of host microprocessor program memory, depending on what features your application uses, plus approximately 0.5 KB for the Pyxos FT Serial API.
    - For more information about code sizings for your firmware applications, see Appendix A in the *Pyxos FT Programmer's Guide*.
- SPI interface:
    - Many microprocessors include an embedded hardware SPI port. Using this port can simplify development.
    - Some low-cost microprocessors do not include an embedded SPI port, or have limited I/O availability. With such microprocessors, you can use a software bit-bang technique to manage serial communications.
    - For more information about the Pyxos FT Chip's SPI interface, see the *Pyxos FT Programmer's Guide*.
- SPI bandwidth:
    - A Pilot transfers a full frame of data (including all read and write timeslots) for each network frame. For continuous mode communications, a Pilot's host microprocessor must able to sustain approximately 200 kbps continuous communication with the Pyxos FT Chip through the SPI interface. For on-demand communications, your application's communications requirements determine the required throughput rate for the host microprocessor's SPI interface. To allow for peak requirements and network overhead, the SPI port should be able to operate at least at 1 Mbps.
    - A Point transfers at most 16 bytes each frame (to read two indexes and to write two indexes). SPI transfer rates that support this requirement range from 5 kbps to 70 kbps, depending on the total number of timeslots in the system. If the Point application does not need to update a full 16 bytes of data for each frame, you can reduce the SPI transfer-rate requirement.
    - See the *Pyxos FT Programmer's Guide* for a description of the Pyxos FT Chip's frame rate requirements.
- Other factors:
    - Power supply – the Pyxos FT Chip requires a 3.3 V power supply. If you select a host microprocessor that also uses a 3.3 V power supply can reduce cost and development effort.
    - Clock – the Pyxos FT Chip provides a 10 MHz clock output that you can use to provide clock input for the host microprocessor.

Design Considerations for the Pyxos FT Chip Clock

As shown in **Figure 9**, the Pyxos FT Chip's XOUT pin requires a 10.5 kΩ pullup resistor between the Pyxos FT Chip and V_{DD3}. Other than the crystal oscillator and this pullup resistor, no other connections should be made to the XIN and XOUT pins.

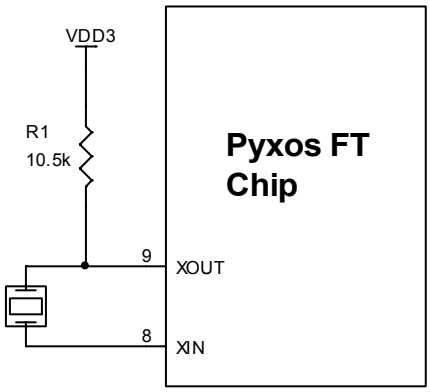

Figure 9. Pullup Resistor for Pyxos FT Chip XOUT Pin

The Pyxos FT Chip presents a capacitance between the XIN and XOUT pins of 16.25 pF. As described in *Pyxos FT Chip Clock* on page 24, the Pyxos FT Chip has been designed to work with an 18 pF parallel resonant crystal. To achieve the overall 18 pF of parallel load capacitance, the XIN and XOUT nets (the traces and vias and surface mount crystal pads) must each have 3.5 pF of capacitance to ground. Two-layer and four-layer printed circuit boards (PCBs) have different trace-to-ground spacings, so this section describes layout considerations for both PCB types.

The layout of the crystal pads and traces for a 4-layer PCB is shown in **Figure 10** on page 34 (the top layer is shown in the figure). **Figure 11** shows the required inner layer stackup. The controlling dimensions listed are in mils (1 mil = 0.001" = 0.39 mm) and in "ounces" of copper for thickness (where 1 ounce = 1.4 mils thickness). The PCB composite is epoxy glass (National Electrical Manufacturers Association (NEMA) grade FR-4) that complies with the European Union Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC), and follows the stackup shown in **Figure 11**.

The outer copper layers start as ½-ounce copper foil, and are subsequently plated to 1-½ ounces (2.1 mils) during the hole-plating process. The final outer-layer thickness has a negligible effect on trace or pad capacitance, and can be changed as necessary for application needs, but the pre-impregnated composite fibre (pre-preg) thickness should be maintained per **Figure 11**.

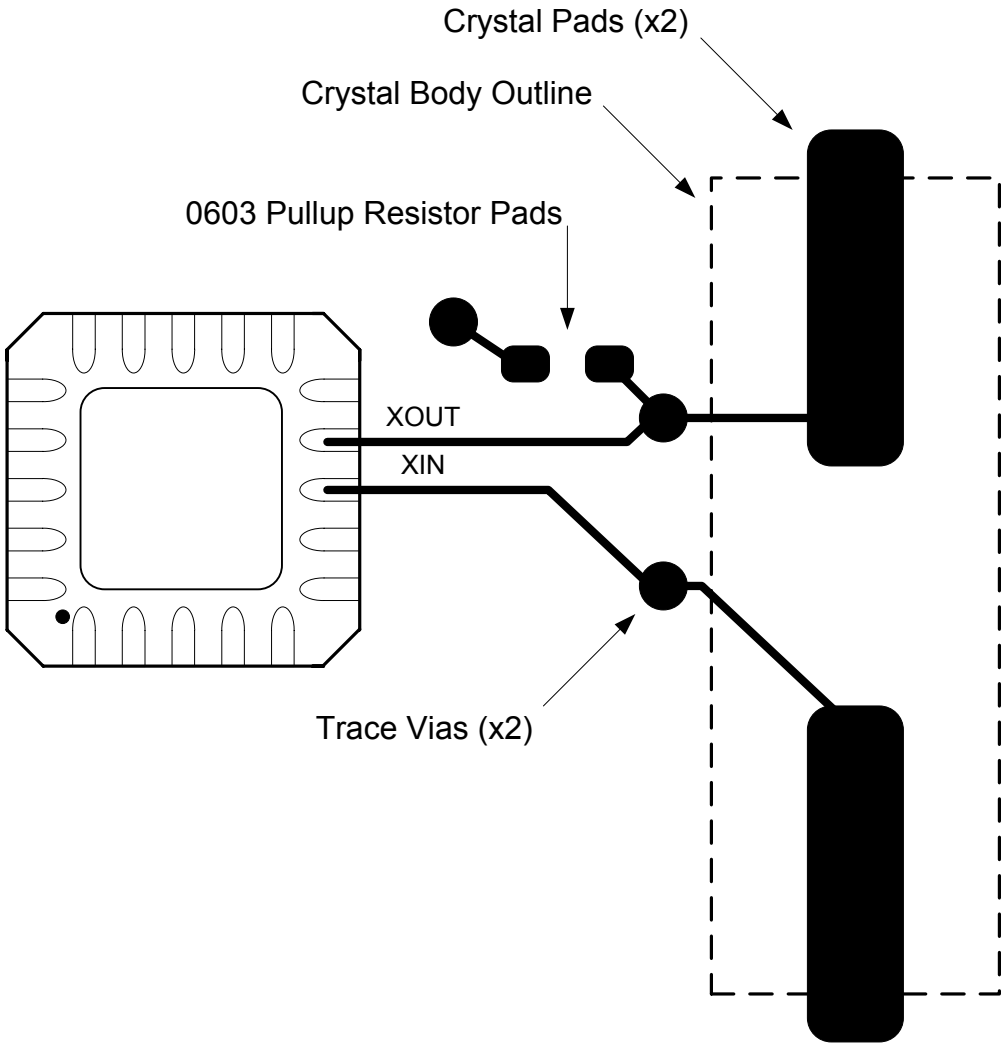

Figure 10. Four-Layer PCB Layout for Crystal (Top View)

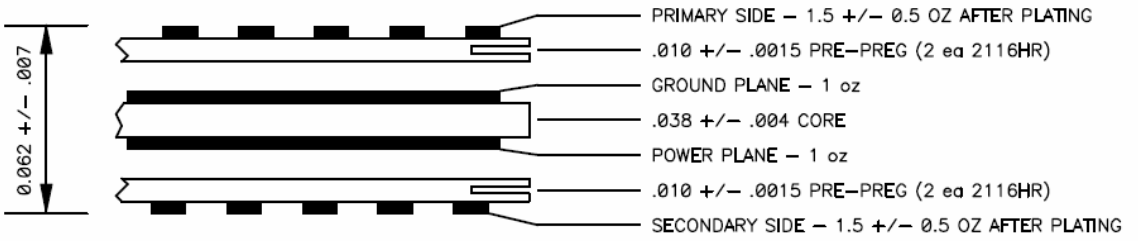

Figure 11. Four-Layer PCB Layer Stackup for Crystal (Side View)

As shown in the layer stackup, the ground layer is adjacent to the top signal layer, spaced 10 mils away by pre-preg. You can achieve the 3.5 pF required capacitance on each of the XIN and XOUT nets with just the standard HC49US crystal surface mount (SMT) pads and relatively short 8 mil wide traces between those pads and the XIN and XOUT pads of the Pyxos FT Chip. For testability, it is traditional to include a via on each net, so that in-circuit test (ICT) fixtures can probe these signals. The pads for the 10.5 kΩ XOUT pullup resistor are shown in the layout as well. The dimensions of these 4-layer PCB features are listed in **Table 7**.

Table 7. Four-Layer PCB Features

Feature	Dimensions
XIN total trace length [1]	290 mils long by 8 mils wide
XOUT total trace length [1]	265 mils long by 8 mils wide
Crystal standard HC49US pads	60 mils wide by 220 mils high
Pullup resistor pads	38 mils wide by 30 mils tall (EIA 0603 standard)
Vias for XIN and XOUT	40 mil pads, 60 mil inner plane clearance

Notes:

1. The total trace length does not include the overlap as the trace goes over the vias and pads.
2. 1 mil = 0.001" = 0.39 mm

The layout of the crystal pads and traces for a 2-layer PCB is shown in **Figure 12** on page 36 (the top layer is shown in the figure). **Figure 13** shows the required inner layer stackup. The controlling dimensions listed are in mils (1 mil = 0.001" = 0.39 mm). The PCB material is made from RoHS-compliant epoxy glass (NEMA grade FR-4), ½-ounce copper-clad laminate, in two layers.

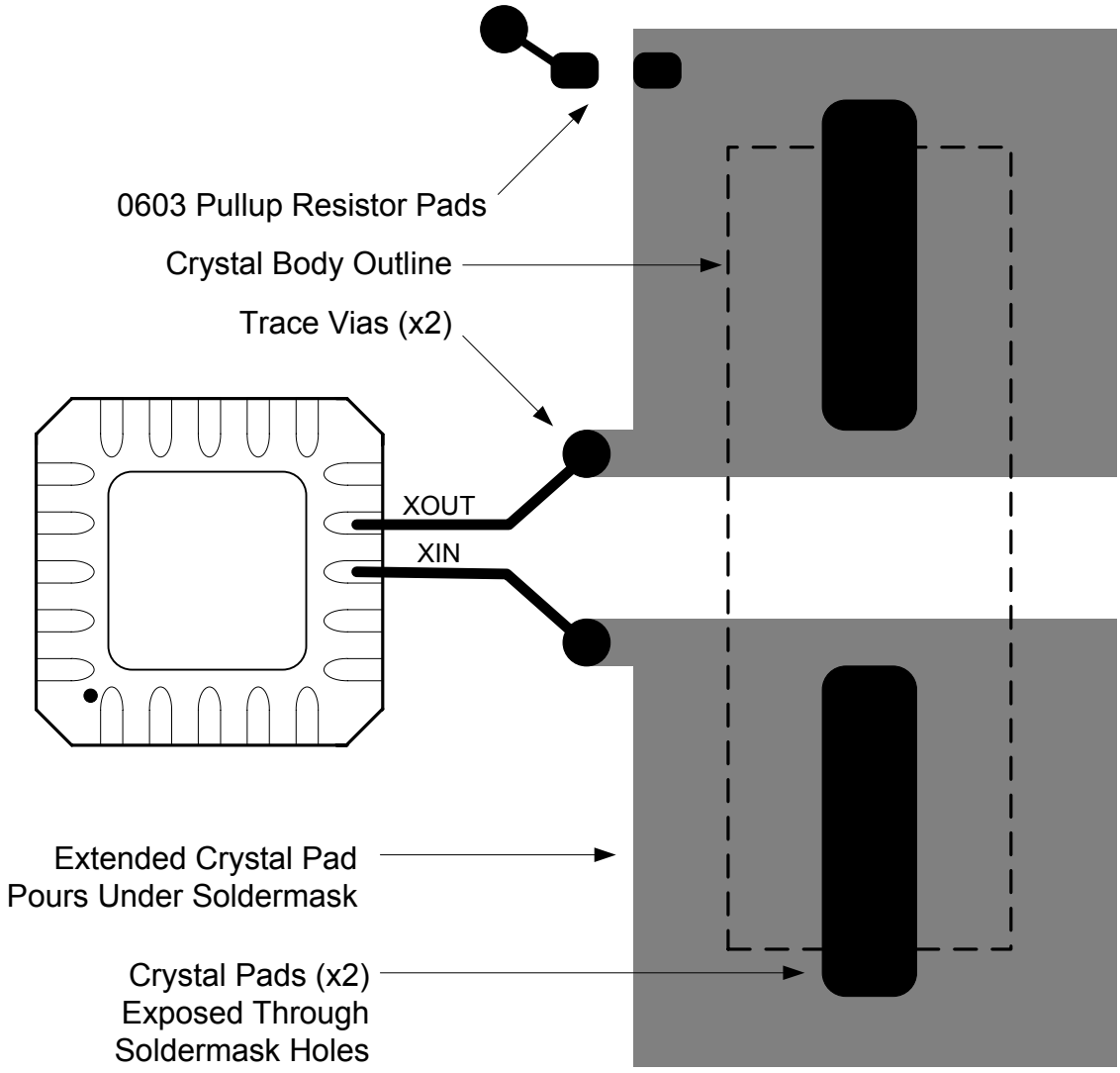

Figure 12. Two-Layer PCB Layout for Crystal (Top View)

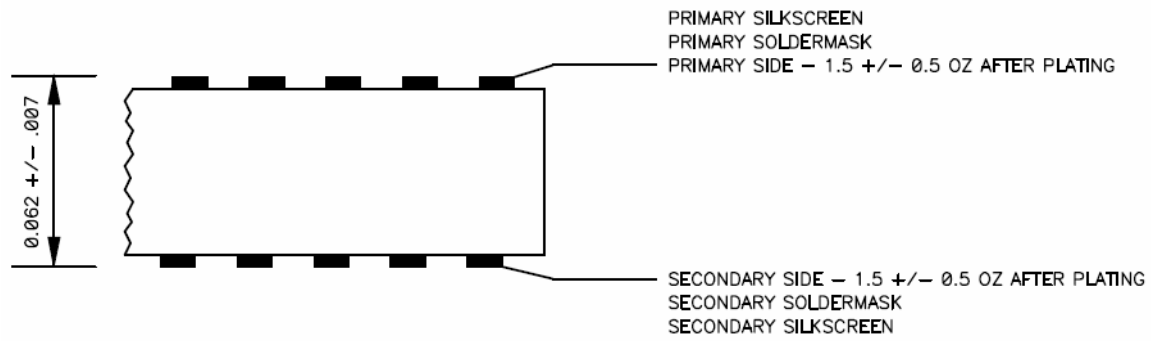

Figure 13. Two-Layer PCB Layer Stackup for Crystal (Side View)

The ground layer for the crystal oscillator circuit is provided by pouring ground on the bottom layer, underneath the Pyxos FT Chip and the crystal pads and traces that are on the top layer. You cannot achieve the 3.5 pF required capacitance on each of the XIN and XOUT nets with just the standard HC49US crystal SMT pads and relatively short 12 mil traces between those pads and the XIN and XOUT pads of the Pyxos FT Chip. You achieve the

extra capacitance by enlarging the pads for the SMT crystal, and only exposing the crystal connection portion of the pads through the soldermask. For testability, it is traditional to include a via on each net, so that in-circuit test (ICT) fixtures can probe these signals. The pads for the 10.5 kΩ XOUT pullup resistor are shown in the layout as well, but the XOUT side of the resistor's pads is placed within the extended crystal pad area, and the correct size opening is placed in the soldermask to expose the connection area for the XOUT side of the pullup resistor. The dimensions of these 2-layer PCB features are listed in **Table 8**.

Table 8. Two-Layer PCB Features

Feature	Dimensions
XIN total trace length [1]	230 mils long by 12 mils wide
XOUT total trace length [1]	270 mils long by 12 mils wide
Crystal standard HC49US pads	325 mils wide by 290 mils high
Pullup resistor pads	38 mils wide by 30 mils tall (EIA 0603 standard)
Vias for XIN and XOUT	40 mil pads

Notes:

1. The total trace length does not include the overlap as the trace goes over the vias and pads.
2. 1 mil = 0.001" = 0.39 mm

Network Coupling Circuits

Pyxos FT networks support four different coupling circuit topologies:

- Direct-connect
- Non-isolated
- Floating
- Transformer-isolated

Each of these coupling circuits provides different levels of protection from electrostatic discharge (ESD) and common-mode interference, as shown in **Table 9** on page 38. In the table, the Node Grounding column uses the following terms:

- Common: The node shares a common ground with the Pyxos FT network.
- Local: The node allows a connection between logic ground and Earth ground.
- Floating: The node's ground floats relative to Earth ground.

In the table, the column for Common Mode Range (DC to 60 Hz) reflects line noise. The column for Common Mode Range (>100 kHz) reflects conducted radio frequency (RF) noise.

See **Table 18** on page 73 for a summary of electromagnetic compatibility (EMC) testing results for each of these coupling types.

Table 9. Summary of Coupling Circuit Types

Coupling Type	Application	Node Power	Node Grounding	Common Mode Range (DC to 60 Hz)	Common Mode Range (>100 kHz)
Direct-connect	Same box	Common	Common	0 V to V_{DD3} (peak)	0 V to V_{DD3} (peak)
Non-isolated	Network	Link power or local power	Local	± 40 V (peak)	1 V_{RMS}
Floating	Network	Link power or local power	Floating	Isolation limit	10 V_{RMS}
Transformer-isolated	Network	Link power or local power	Local	277 V_{RMS}	10 V_{RMS}

The following sections describe each of the coupling types.

Direct-Connect

A direct connection to the Pyxos FT network is appropriate for applications with the following characteristics:

- Low impedance common ground
- Common power supply
- Limited distance between devices

An advantage to using direct-connect is that you do not need any off-chip coupling components. Thus, you can connect the Pyxos FT Chip directly to the differential network.

Figure 14 shows an example of a direct connection to the Pyxos FT network.

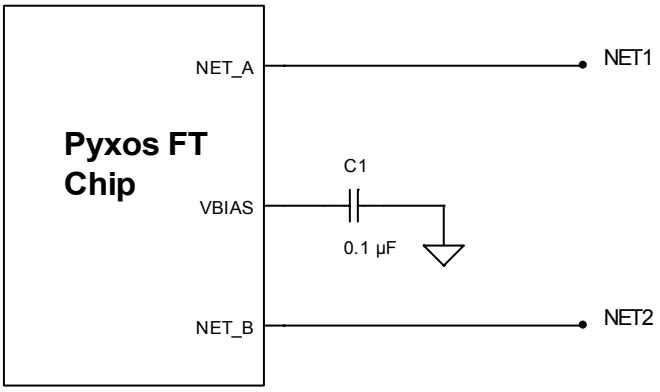

Figure 14. Direct-Connect Topology

You can use direct-connect topology when all Pyxos FT devices on the network share a common ground and power supply, and the voltage differential between the ground points of

the devices is small (less than approximately 100 mV). This coupling method is suitable for applications where all of the devices are in a single box, within 5 m of each other.

Because the Pyxos FT Chip provides sufficient ESD protection for most applications, you generally do not need to include ESD diodes for the NET_A or NET_B pins. See Chapter 7, *Design and Test for Electromagnetic Compatibility*, on page 63, for more information about designing for ESD protection.

Non-Isolated

Because the communications signals in a Pyxos FT network do not use energy below 100 kHz, you can use a coupling circuit that filters out noise in the 50 to 60 Hz range, where the largest amplitude noise is likely to be found.

Figure 15 shows an example of non-isolated coupling to the Pyxos FT network. **Table 10** lists the coupling components needed for both the non-isolated and floating topologies.

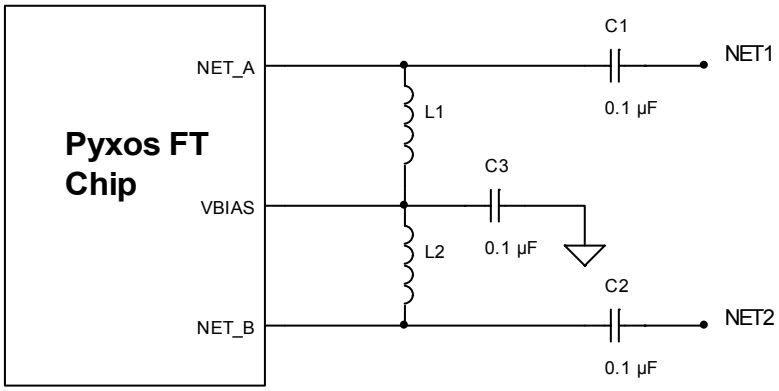

Figure 15. Non-Isolated Topology

You can use non-isolated topology when a device is connected to Earth ground and the common mode rejection requirement is low, that is, the high-frequency common-mode noise is 1 V_{RMS} or less.

Table 10. Parts for Non-Isolated and Floating Topologies

Part	Value	Required Specifications	Example Vendor Part Number
C1, C2, C3	0.1 µF	±10% ≥ 100 V X7R	Vishay VJ1206Y104KXBTW1BC or Kemet C1206C104K1RACTU
L1 and L2 (without link power)	1 mH	±10% ≥ 15 mA DC rated current ≤ 25 Ω DC resistance	Taiyo Yuden LB2518T102
L1 and L2 (with link power)	≥ 1.5 mH	±10% ≥ 15 mA DC rated current ≤ 25 Ω DC resistance	One Taiyo Yuden LHL08TB-152J or Two Taiyo Yuden LB2518T102

Part	Value	Required Specifications	Example Vendor Part Number
Note: For link-powered devices, the inductors L1 and L2 can be either a single 1.5 mH LHL08TB-152J inductor or two 1 mH LB2518T102 inductors in series. Two LB2518T102 inductors are physically smaller than a single LHL08TB-152J inductor.			

Floating

If the noise requirements of your application require that the Pyxos FT device float relative to Earth ground, you can use a floating topology. This topology serves the same function as the non-isolated topology, but the device floats relative to Earth ground. Because the device floats, this type of coupling provides high common-mode rejection performance. For more information about EMC requirements, see Chapter 7, *Design and Test for Electromagnetic Compatibility*, on page 63.

Figure 16 shows an example of a floating topology. **Table 10** lists the coupling components needed for both the non-isolated and floating topologies.

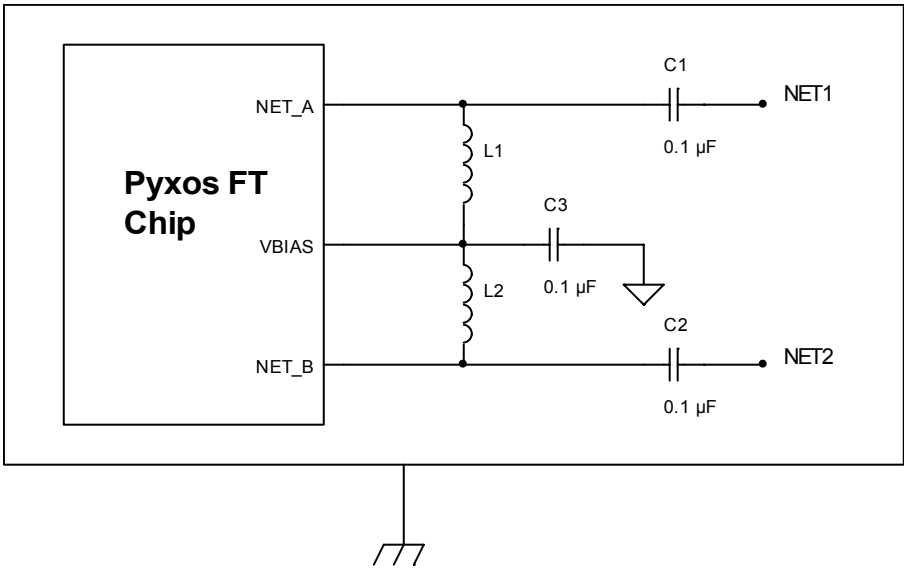

Figure 16. Floating Topology

You can use floating topology when the device is already isolated (such as in a light switch, thermostat, and so on) and the Pyxos FT Points are link powered or have an isolated power supply.

Transformer-Isolated

Transformer-isolated topology isolates common-mode noise, up to 277 V_{RMS} from DC to 60 Hz, and up to 10 V_{RMS} from 150 kHz to 80 MHz (equivalent to IEC 61000-4-6 level 3).

Use the transformer-isolated topology when the device must be Earth grounded, and when high common-mode rejection is required.

Figure 17 shows an example of a transformer-isolated topology. **Table 11** lists the coupling components needed for the transformer-isolated topology.

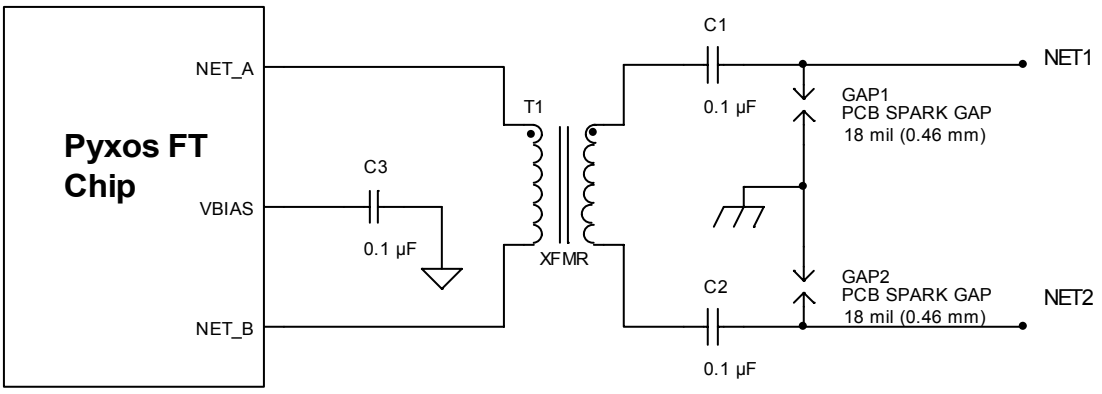

Figure 17. Transformer-Isolated Topology

Table 11. Parts for Transformer-Isolated Topology

Part	Value	Required Specifications	Example Vendor Part Number
C1, C2, C3	0.1 µF	±10% ≥ 100 V X7R	Vishay VJ1206Y104KXBTW1BC or Kemet C1206C104K1RACTU
T1	1:1 turn ratio	Custom	Transtek TMS80040CS

Power Supply

For each Pyxos FT device, you have two power supply options:

- Local power: provide power from a power source that is local to the device
- Link power: provide power over the Pyxos FT network

For local power, you can use any power supply that can provide 3.3 VDC ±10%, with output ripple of less than 50 mV_{pp} with a 20 MHz bandwidth.

For link power, you have two types of power supply designs that you can use for the Pyxos FT device:

- DC-DC switching power supply
- Linear power supply

The two power supply designs for link power are described in *Node Power Supply for Link Power* on page 57.

LonWorks Connectivity

In addition to managing a Pyxos FT network, a Pyxos FT Pilot can also communicate with LONWORKS devices over a LONWORKS network. To provide LONWORKS connectivity, the Pyxos FT Pilot needs to provide a LONWORKS Gateway, which includes either a Neuron Chip with a ShortStack Micro Server or an FT 3150 Smart Transceiver. The Pilot's firmware application program also needs to include appropriate calls to the ShortStack API and encapsulate Pyxos Network Variable (PNV) updates as LONWORKS Network Variables.

For an example LONWORKS Gateway, refer to the Pyxos FT EVK and the *Pyxos FT EVK User's Guide*. For more information about the ShortStack Micro Sever, see the *ShortStack User's Guide*; for more information about the FT 3150 Smart Transceiver, see the *FT 3120 / FT 3150 Smart Transceiver Databook*.

Providing LONWORKS connectivity is optional.

Layout Guidelines

Figure 18 on page 43 shows a portion of the top layer of a 4-layer printed circuit board (PCB) layout for the Pyxos FT Chip, along with the other building blocks of a PCB design. The Pyxos FT chip layout shown uses T101 for its transformer-isolated network coupling circuit.

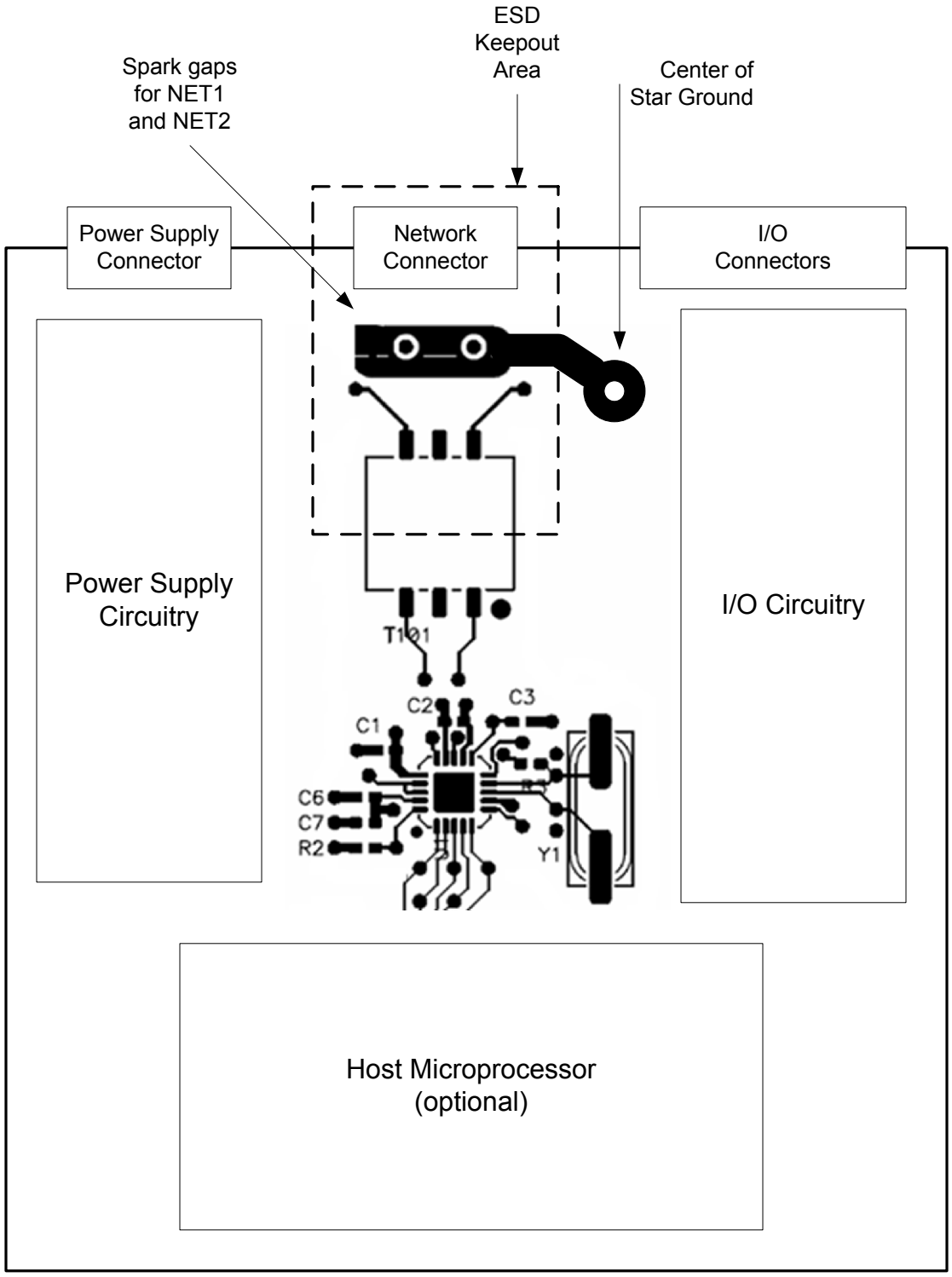

Figure 18. Example PCB Layout Design

Electrostatic discharge (ESD) and electromagnetic interference (EMI) are two of the most important design considerations for a device's PCB layout. Tolerance of ESD and other types of network transients requires careful layout for the power, ground, and other device circuitry. In general, ESD discharge currents return to Earth ground or to other nearby metal structures. The device's ground scheme must be able to pass this ESD current

between the network connection and the device's external ground connection without generating significant voltage gradients across the device's PCB. The low inductance star-ground configuration shown in **Figure 18** accomplishes this task.

The star-ground configuration conducts transients out of the device with minimal disruption to other function blocks. For more information about the benefits of a star-ground configuration, see *Achieving High Immunity* on page 65. The following list describes the features of the design layout shown in **Figure 18**:

Star Ground Configuration: The various blocks of the device that directly interface with off-board connections (the network, any external I/O, and the power supply cable) are arranged so that the connections are together along one edge of the PCB. This arrangement allows any transient current that comes in by one connection to flow back out of the device by one of the other connections.

If connection is made between the PCB ground and a metal enclosure, that connection should be made using a low-inductance connection (like a short standoff) in the center of the star ground. This is illustrated by the standoff hole shown in **Figure 18**. The center of the star ground is anywhere within the common ground area around the off-board connections.

For a 4-layer PCB, the ground plane serves to distribute ground from the center of the star ground out to the various function blocks in the floorplan.

For a 2-layer PCB, ground pours should be placed on the bottom layer (and also on the top layer where possible) in order to connect the grounds of the various function blocks to the center of the star ground.

Sparkgaps for Transformer-Isolated Devices: The PCB spark gaps shown are used to protect the Pyxos FT communication transformer from arcing through. Pyxos FT devices that use the direct-connect or the non-isolated coupling options do not need the PCB spark gaps. The dimensions for the spark gaps are shown in **Figure 19** on page 45. These dimensions provide an 18 mil (0.018" or 0.46 mm) circular air gap on the top layer of the PCB, as long as the top soldermask layer is pulled back from the gap as shown, to expose the ground portion of the gap. The board finish for the outer layer exposed pads of the spark gap require immersion silver plating, such as Enthone AlphaSTAR® immersion silver, with a 9 to 15 microinch (229 to 381 nm) finished thickness.

Figure 19 shows a side view of the gap in a 2-layer or 4-layer PCB. For a 4-layer PCB, the internal layers are cleared away from the area around the spark gaps and NET1/NET2 traces. See the discussion below about this ESD keepout area. The center conductor (via) of the spark gaps is connected to NET1 and NET2, as shown in the transformer-isolated coupling circuit in **Figure 17** on page 41. The surrounding ground plane on the top layer is connected to Earth ground or to logic ground. If Earth ground is separate from logic ground, then a capacitor should be used to tie Earth ground to logic ground at the center of the star ground.

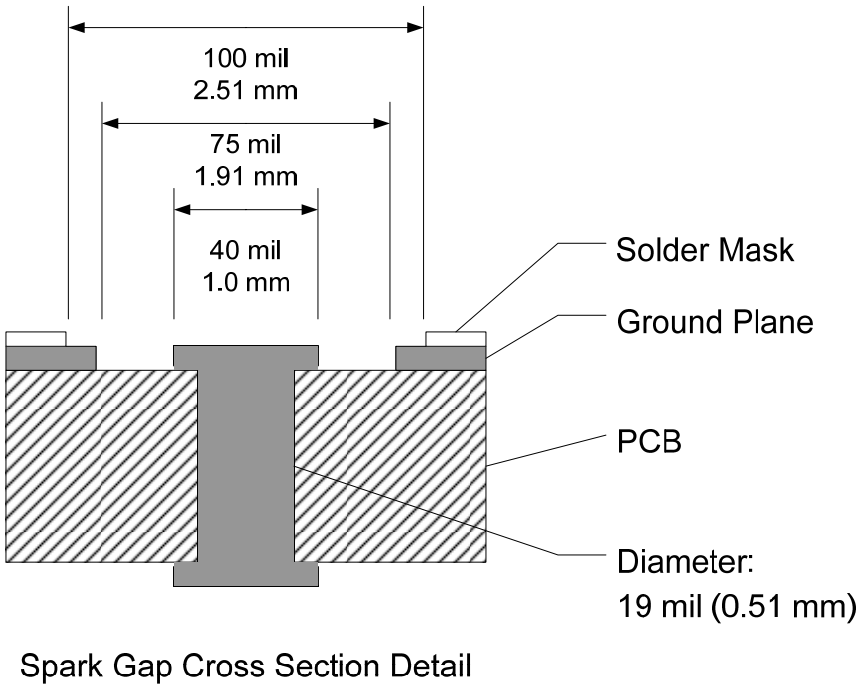

Figure 19. PCB Spark Gap Cross Section Detail

ESD Keepout Area: For devices that use the transformer-isolated coupling circuit, the area around the Pyxos FT network connection traces and components should be considered "ESD Hot", and other traces and components (and inner planes) should be kept at least 0.25" (6.4 mm) away from them to prevent ESD arc-overs to anything other than the top layer ground area around the spark gaps.

This top layer ground should have a low-inductance return to an external metal package if there is one (as afforded by the standoff shown in **Figure 18**). If there is no metal package, then this top-layer ground area should connect to the ground areas near the power supply connector and the external I/O connectors, as applicable.

The transient current that is clamped by the spark gaps should be routed off of the PCB as directly as possible, without any opportunity to run through the Pyxos FT Chip itself, and any other circuitry, such as the host microprocessor.

Ground Return for Pyxos FT Chip: The Pyxos FT Chip has internal protection circuitry built into its NET_A, NET_B, and VBIAS pins. When an ESD or surge transient comes in from the network, the portion of the transient that makes it to the Pyxos FT Chip is clamped to the chip's V_{DD3} and ground pins. V_{DD3} is bypassed to ground at the Pyxos FT Chip, so the transient current returns to the center of the star ground through the ground layer for a 4-layer PCB, or the ground pours for a 2-layer PCB. Be sure to provide a short and wide ground path from the Pyxos FT Chip back to the center of the star ground. For the non-isolated or direct-connect coupling options, you can move the Pyxos FT Chip closer to the network connector than shown in **Figure 18**.

Host Microprocessor Kept Away From Network Connection: The (optional) host microprocessor is a potential source of digital noise that could cause radiated EMI problems if that noise is allowed to couple onto the external network, power, or I/O wiring. To help prevent this, the host microprocessor and any other noisy digital circuitry should be kept away from the network side of the Pyxos FT Chip. The

floorplan shown in **Figure 18** shows the host microprocessor placed on the opposite edge of the PCB from the network, power, and I/O connectors.

V_{DD3} Decoupling Capacitors: A good rule of thumb is to provide at least one V_{DD3} decoupling capacitor to ground for each V_{DD3} power pin on an IC in the design. For SMT devices like the Pyxos FT Chip, each decoupling capacitor should be placed on the top layer with the chip, and placed as close as possible to the chip to minimize the length of V_{DD3} trace between the capacitor and the chip's V_{DD3} pad. The ground end of the capacitor should have a wide, short connection to ground. Keeping these connections short and wide reduces their inductance, which improves the effectiveness of the decoupling. SMT capacitors with a value of 0.1 µF work well for decoupling, as long as the connections are kept very short. If you use ESD clamp diodes between V_{DD3} and ground on I/Os, there should generally be at least one decoupling capacitor for every two diode clamps, placed very close to those diode clamps.

5

Pyxos FT Communications

This chapter describes cabling and termination for Pyxos FT networks.

Network Cabling

A Pyxos FT network can use either of the following cable types:

- Belden® 8471 unshielded cable (or equivalent American wire gauge (AWG) 16 (1.3 mm) twisted-pair wire)
- AWG 24 (0.511 mm) ANSI/TIA/EIA-568-B.2-2001 Category 5 twisted-pair wire

You can choose the cable type that is most appropriate for your Pyxos FT network application, based on cost, performance, and availability of the different cable types.

The network connection (NET1 and NET2) is polarity insensitive. Therefore, either of the two wires of the twisted pair can be connected to either of these network connections.

For either cable type, the average temperature of the wire must not exceed +55 °C, although individual segments of wire can be as hot as +85 °C.

As a general rule, Pyxos FT network channel communication cables should be separated from high voltage power cables. Follow local electrical codes with regard to cable placement.

The following sections describe the characteristics of the two cable types.

Belden 8471 Cable

Belden publishes some but not all of the cable parameters that affect signaling on Pyxos FT channels. Echelon has measured additional important parameters for this cable. The following list defines the important characteristics for this cable:

- Wire diameter: AWG 16 (1.3 mm)
- DC resistance R_{loop}: 29 Ω/km
- Mutual capacitance: 54 nF/km
- Magnitude of the characteristic impedance $|Z_0|$: 103 Ω @ 250 kHz
- Propagation delay: 5.6 µs/km

For a Pyxos FT network operating in a bus topology, the maximum bus length of Belden 8471 cabling is 400 meters, with a maximum stub length of 0.3 meters.

For a Pyxos FT network operating in free topology, the maximum length of Belden 8471 cabling is 100 meters maximum total wire length.

For a Pyxos FT network operating with link power, see *Distance Limitations for Link Power* on page 58 for information about maximum cable lengths.

ANSI/TIA/EIA 568-B Category 5 Cable

The specifications for Category 5 cabling are defined by the Telecommunications Industry Association standard 568B. The parameters for this cable include:

- Wire diameter: AWG 24 (0.511 mm)
- DC resistance R_{loop}: ≤ 188 Ω/km @ 20 ºC
- Mutual capacitance: ≤ 66 nF/km
- Magnitude of the characteristic impedance $|Z_0|$: 100 Ω @ 1 MHz (~110 Ω @ 250 kHz)

- Propagation delay: ≤ 6.1 µs/km @ 20 ºC

Echelon has qualified cabling that meets the TIA 568B standard, and any cabling – from any manufacturer – that meets this standard is acceptable.

For a Pyxos FT network operating in a bus topology, the maximum bus length of Category 5 cabling is 400 meters, with a maximum stub length of 0.3 meters.

For a Pyxos FT network operating in free topology, the maximum length of Category 5 cabling is 100 meters maximum total wire length.

For a Pyxos FT network operating with link power, see *Distance Limitations for Link Power* on page 58 for information about maximum cable lengths.

Network Termination

Pyxos FT networks require termination for proper data transmission performance. The type of terminator varies depending on whether the network is configured as a free-topology network or a bus-topology network. The following sections describe the required terminators and termination procedures.

The network terminator that you use depends only on the network topology; it does not depend on whether your network transmits power as well as communications signals (that is, if devices are locally powered or link powered).

Caution: Do not use Echelon 44100 or Echelon 44101 network terminators for your Pyxos FT network. Because the power transmission characteristics for a Pyxos FT network are different than those of a TP/FT-10 channel, using the Echelon 44100 or Echelon 44101 network terminators in a Pyxos FT network can damage the terminators and damage the network cable.

Termination for a Free-Topology Network

For a free-topology network, a single network termination is required. The terminator can be placed anywhere on the free topology network. **Figure 20** shows the network termination circuit. **Table 12** lists the components for the circuit.

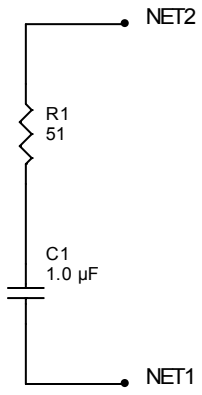

Figure 20. Network Terminator for Free-Topology Network

The network connection (NET1 and NET2) is polarity insensitive. Therefore, either of the two wires of the twisted pair cable can be connected to either of these network connections.

Table 12. Parts for Free-Topology Network Terminator

Part	Value	Required Specifications	Example Vendor Part Number
R1	51 Ω	±5% 1/2 W Carbon composition	Ohmite OF510J (axial)
C1	1.0 µF	±10% ≥ 100 VDC Metal polyester	Panasonic ECQE1105KF (radial)

Recommendation: Use a carbon composition resistor for the resistor (R1) and a metal polyester capacitor for the capacitor (C1) in the network terminator because they provide more robust protection from network surges than metal-film resistors and ceramic capacitors.

Termination for a Bus-Topology Network

In bus-topology network, two terminations are required, one at each end of the bus. **Figure 21** shows the network termination circuits. **Table 13** lists the components for the circuit.

A doubly terminated bus can have stubs of up to 0.3 meters from the bus to each device.

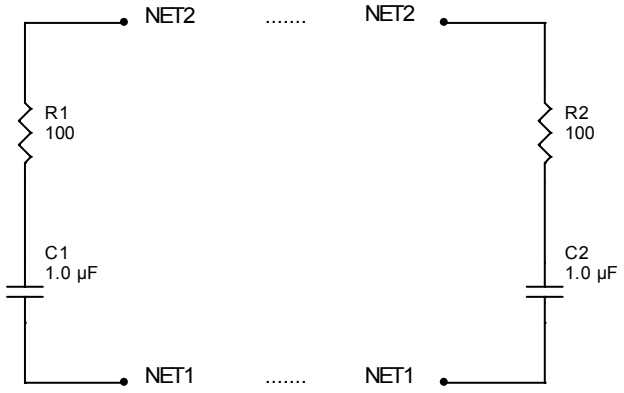

Figure 21. Network Terminators for Bus-Topology Network

The network connection (NET1 and NET2) is polarity insensitive. Therefore, either of the two wires of the twisted pair cable can be connected to either of these network connections.

Table 13. Parts for Bus-Topology Network Terminator

Part	Value	Required Specifications	Example Vendor Part Number
R1 and R2	100 Ω	±5% 1/2 W Carbon composition	Ohmite OF101J (axial)

Part	Value	Required Specifications	Example Vendor Part Number
C1 and C2	1.0 µF	±10% ≥ 100 VDC Metal polyester	Panasonic ECQE1105KF (radial)

Recommendation: Use a carbon composition resistor for the resistors (R1 and R2) and a metal polyester capacitor for the capacitors (C1 and C2) in the network terminators because they provide more robust protection from network surges than metal-film resistors and ceramic capacitors.

6

Link Power

This chapter describes link power for Pyxos FT networks, including the requirements for the source power supply and node power supply, and how link power affects overall network wire distances.

Overview

There are two ways that devices within a Pyxos FT network can receive power:

- From a power supply and power source attached directly to the device
- From the Pyxos FT network cable

When a device receives power over the Pyxos FT network cable, it is receiving *link power*. In this case, the device receives both communications data and power over the same physical wires, which eliminates the need for separate wiring. A Pyxos FT network can include a mixture of devices that are locally powered and link powered.

One device in the Pyxos FT network connects to the AC mains power and contains the network *source power supply*. Which device contains the source power supply depends on your application: it could be the Pilot, one of the Points, or a separate device (such as the plug-in power adapter). Each of the other devices in the Pyxos FT network receives its power from the network and contains a *node power supply*. The source and node power supplies have different requirements, as described in the sections *Source Power Supply* on page 55 and *Node Power Supply for Link Power* on page 57.

The source power for a link-powered Pyxos FT network can be either 24 VAC (50–60 Hz) or 24 VDC. Each link powered device receives 24 V (AC or DC) over the network.

Note that link power is not the same as Echelon's power line technology, that is, you cannot connect the Pyxos FT network directly to the AC power mains. The Pyxos FT network is connected to each Pyxos FT device, and the link power is delivered over the network.

Figure 22 shows a block diagram of a source power supply and filter connected to a Pyxos FT network and a link-powered Point connected to the network. The source power supply could be a DC supply or an AC supply. For the link-powered Point, the high-pass filter presents the communications signals to the Pyxos FT Chip, and the low-pass filter removes the communications signals from the power input to the node power supply. These filters are described in the following sections.

The network connection is polarity insensitive. Thus, the figure does not distinguish between the two wires of the twisted pair cable that are connected to the network connections.

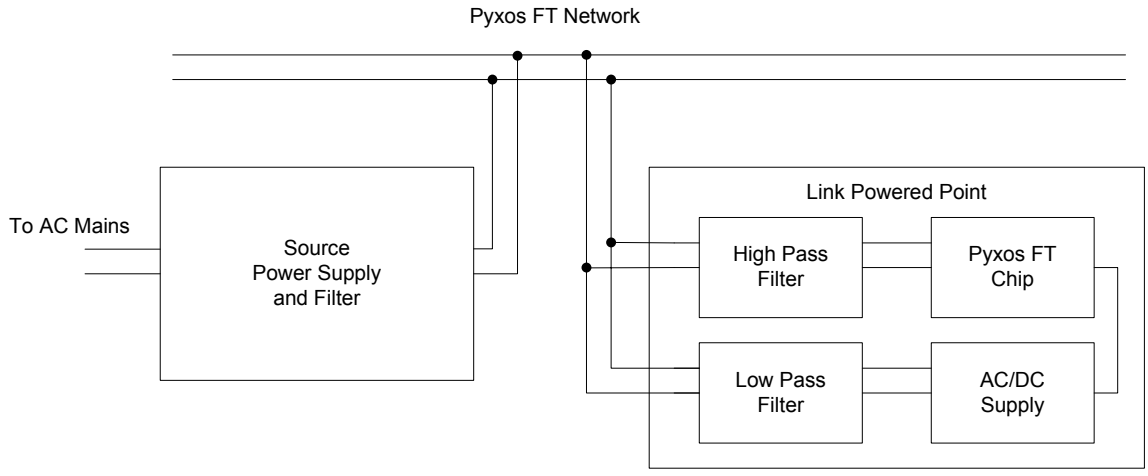

Figure 22. Link-Powered Point Connected to a Pyxos FT Network

Because of the resistance inherent in the twisted-pair wire that the Pyxos FT network uses for communication and link power transmission, there are distance limitations for devices within a link-powered Pyxos FT network. These limitations are described in *Distance Limitations for Link Power* on page 58.

The specific designs of the power system and of the power supplies are dependent on your Pyxos FT application; however, Appendix B, *Reference Designs*, on page 91, describes reference designs that show how to isolate the power from the communications signals.

Source Power Supply

For the power input to the Pyxos FT network, you have two options: AC source power and DC source power. The AC source power supply connects to the AC mains and provides a line filter and step-down transformer. DC source power can be drawn from a 24 VDC power supply with an output filter.

AC Source Power

For 24 VAC source power, the source-power supply is simply an AC line filter followed by an appropriate step-down power transformer, as shown in **Figure 23**. For the line filter, you must use a Schaffner FS23488-3-06 one-stage filter, which provides both filtering and surge protection for the network.

For the power transformer, you can use any 24 VAC transformer that meets your application needs. In a Pyxos FT network of 32 devices that each use more than 35mA of application current (that is, 32 total PULs; see *Distance Limitations for Link Power* on page 58 for the definition of a PUL), the transformer rating should be 55 VA or better; you can scale down this rating for networks with fewer PULs.

The secondary leakage inductance for the transformer should be 950 µH or greater to provide sufficient inductance for the network. See *Testing Transformer Leakage Inductance* on page 56 for a description of how to test the secondary leakage of a transformer.

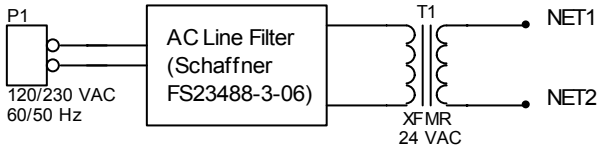

Figure 23. AC Source Power Supply

DC Source Power

For a DC power supply, you can integrate the filter into the design of the output stage of the supply to make it more economical. Or you can add a filter circuit for an off-the-shelf DC power supply, as shown in **Figure 24** on page 56. **Table 14** lists the components for the circuit.

For the 24 VDC source power supply, you can use any off-the-shelf supply with the following characteristics:

- Output voltage: 24 VDC ±10%
- Output current: ≥ 2.1 A
- Output ripple: ≤ 240 mV_{pp} for 20 MHz bandwidth

In a Pyxos FT network of fewer than 32 devices that each use less than 35 mA of application current (that is, fewer than 32 total PULs; see *Distance Limitations for Link Power* on page 58 for the definition of a PUL), you can scale down the output current requirement for the power supply.

The output filter raises the impedance at communication frequencies and reduces the power-supply noise on the network. For the inductors shown in the figure, you can use a high current toroid inductor, such as a Bourns/J.W. Miller 2322-H-RC inductor.

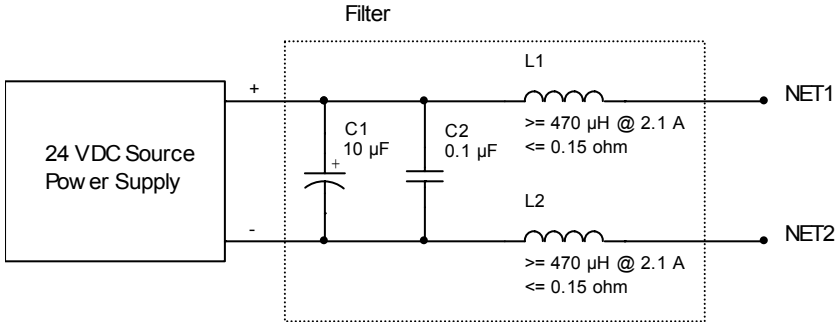

Figure 24. DC Source Power Supply

Table 14. Parts for DC Source Power Supply

Part	Value	Required Specifications	Example Vendor Part Number
C1	10 µF	±10% ≥ 100 VDC Metal polyester	Panasonic ECA2AHG100 (radial)
C2	0.1 µF	±10% ≥ 100 VDC Metal polyester	Panasonic ECQE1104KF (radial)
L1 and L2	≥ 470 µH	2.1 A ≤ 0.15 Ω [0]	Bourns/J.W. Miller 2322-H-RC
Note: The required specification for the inductors L1 and L2 must be ≤ 0.15 Ω for a Pyxos FT network with 32 devices that each use more than 35mA of application current (that is, 32 total PULs; see *Distance Limitations for Link Power* on page 58 for the definition of a PUL); in a network with fewer PULs, you can scale up this value.			

Testing Transformer Leakage Inductance

A transformer's leakage inductance is an inductive component that is attributable to any magnetic flux that does not sufficiently link the primary to the secondary windings. Leakage inductance is effectively an inductor in series with the primary and secondary circuits. The AC source power supply shown in **Figure 23** on page 55 requires a minimum value of leakage inductance to ensure that the transformer does not excessively load the Pyxos FT network at communication frequencies.

To measure the leakage inductance, apply a short circuit to the primary winding while you measure the voltage drop across the secondary winding, as shown in **Figure 25**.

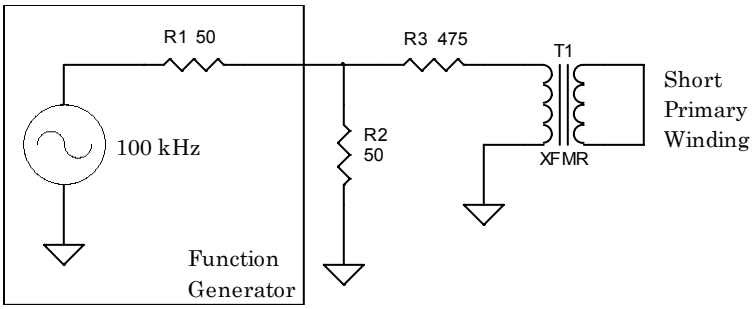

Figure 25. Simple Transformer Leakage Test

The following parameters characterize this test:

- Use a 50 Ω function generator set to 1 V_{pp} at 100 kHz
- Connect the function generator to two resistors and the transformer under test
- Short the primary winding of the transformer
- Measure the voltage across the secondary winding of the transformer

The measured secondary voltage must be > 0.78 V_{pp} to supply sufficient inductance for a Pyxos FT network.

Node Power Supply for Link Power

Input power for the node power supply can be either AC or DC. Appendix B, *Reference Designs*, on page 91, provides two reference designs for node power supplies.

For each powered device within your Pyxos FT network, you need to include an isolator filter circuit, as shown in **Figure 26**. The filter circuit is a simple inductor-capacitor (LC) filter that is designed to:

- Provide high impedance at data communication frequencies to filter out the communication signals
- Allow the low frequency power (DC or 50–60 Hz AC) to flow to the devices

Because the filter passes significantly lower currents than the filter for the source power supply, node power supply inductors can be fairly small and inexpensive.

In addition to the filter, you need to provide a full-wave bridge to provide polarity insensitivity for 24 VDC networks, as shown in **Figure 33** on page 93 and **Figure 38** on page 98. **Table 15** on page 58 lists the components needed for the node power supply filter circuit.

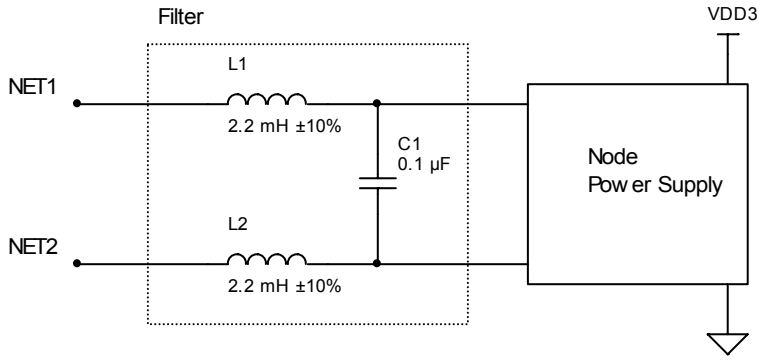

Figure 26. Node Power Supply Filter

Table 15. Parts for Node Power Supply Filter

Part	Value	Required Specifications	Example Vendor Part Number
L1 and L2	2.2 mH	±10% ≥ 80 mA DC rated current ≤ 12 Ω DC resistance	Taiyo Yuden LHL08TB-222J
C1	0.1 µF	±10% ≥ 100 VDC X7R	Vishay VJ1206Y104KXBTW1BC or Kemet C1206C104K1RACTU

Node Power Supply Reference Designs

For the node power supply, you can use either of the designs that are described in Appendix B, *Reference Designs*, on page 91:

- A switching power supply
- A linear power supply

Table 16 compares the basic characteristics of these two designs. Appendix B describes these designs in detail.

Table 16. Characteristics of the Node Power Supply Designs

Parameter	Switching Power Supply	Linear Power Supply
Input Voltage Range	8.5 V to 40 V	8.5 V to 40 V
Output Voltage	3.3 V ± 10%	3.3 V ± 10%
Maximum Application Current	100 mA	15 mA

Distance Limitations for Link Power

For a link-powered Pyxos FT network, each device represents a load on the link power supply. The node power supply for each device supplies application current (for components external to the Pyxos FT Chip): up to 100 mA for a switching power supply or up to 15 mA for a linear power supply.

Several factors can influence the distance limitations for link power networks, including:

- The size of the wire used for the network:
  - AWG 16 (1.3 mm) twisted-pair wire (Belden 8471 unshielded cable)
  - AWG 24 (0.511 mm) ANSI/TIA/EIA-568-B.2-2001 Category 5 twisted-pair wire
- Whether the network uses bus topology or free topology
- Whether the source power is AC or DC
- The total power drawn by all of the devices on the network

- The average distance of the devices from the source power
- The distribution of the devices on the network

To aid the discussion of how network cable distance and power consumption are related, a standard unit of power load is defined, the *Power Unit Load* (PUL):

- 1 PUL represents a Pyxos FT device that requires between 35 mA and 100 mA of application current from its switching power supply.
- ½ PUL represents a Pyxos FT device that requires no more than 35 mA of application from its switching power supply, or up to 15 mA of application current from its linear power supply.

Although an individual device typically uses less than the maximum application current that is available from its node power supply, for this discussion, a device requires either 1 PUL or ½ PUL.

In general, as you increase the number of devices (the number of PULs) on the network, you decrease the distance that each device can be from the source power. This decrease represents the power losses due to the resistance of the wire. That is, as you increase the distance of the devices from the source power, you decrease the number of devices that the network can include.

The relationship between distance and PUL is shown in **Table 17**. The table includes columns for the device distances in different environments: with an AC or DC source power supply, in either a bus or free topology network, and using either AWG 16 cable or Category 5 cable. For a bus topology, the values in the table represent the maximum average distance for all of the PULs from their source power supply, in meters. For a free topology, the values in the table represent the maximum average distance for PULs on a particular branch of the network extending out from the source power supply, in meters.

For example, for the PUL value of 12, the maximum average distance for all PULs in a bus topology network from the source power supply is 208 m for an AC source power supply with AWG 16 wire, but the maximum average distance for PULs on a particular network branch in a free topology network is 100 m for the same AC source power supply with the same AWG 16 wire (however, because the communication distance limit for a free topology network is 100 m, a Pyxos FT network cannot contain more than one 100 m branch), and so on across the row.

Table 17. Maximum Average Distance from Source Power to Link-Powered Devices

	AWG 16 (1.3 mm) Twisted-Pair Cable				AWG 24 (0.511 mm) Category 5 Cable			
	Bus Topology		Free Topology		Bus Topology		Free Topology	
PULs	AC	DC	AC	DC	AC	DC	AC	DC
1	400 m	400 m	100 m	100 m	400 m	400 m	100 m	100 m
2	400 m	400 m	100 m	100 m	237 m	268 m	100 m	100 m
3	400 m	400 m	100 m	100 m	156 m	178 m	95 m	100 m
4	400 m	400 m	100 m	100 m	115 m	133 m	71 m	100 m
5	400 m	400 m	100 m	100 m	91 m	106 m	57 m	99 m

	AWG 16 (1.3 mm) Twisted-Pair Cable				AWG 24 (0.511 mm) Category 5 Cable			
	Bus Topology		Free Topology		Bus Topology		Free Topology	
PULs	AC	DC	AC	DC	AC	DC	AC	DC
6	400 m	400 m	100 m	100 m	74 m	88 m	47 m	82 m
7	383 m	400 m	100 m	100 m	63 m	75 m	40 m	70 m
8	330 m	400 m	100 m	100 m	54 m	66 m	35 m	61 m
9	289 m	354 m	100 m	100 m	47 m	58 m	31 m	55 m
10	256 m	319 m	100 m	100 m	42 m	52 m	28 m	49 m
11	229 m	289 m	100 m	100 m	37 m	47 m	26 m	44 m
12	208 m	263 m	100 m	100 m	34 m	43 m	24 m	41 m
13	188 m	243 m	100 m	100 m	31 m	40 m	22 m	38 m
14	172 m	225 m	100 m	100 m	28 m	37 m	20 m	35 m
15	158 m	209 m	100 m	100 m	26 m	34 m	19 m	32 m
16	145 m	195 m	100 m	100 m	24 m	32 m	17 m	30 m
17	135 m	183 m	100 m	100 m	22 m	30 m	16 m	29 m
18	125 m	172 m	96 m	100 m	20 m	28 m	16 m	27 m
19	116 m	163 m	91 m	100 m	19 m	37 m	15 m	26 m
20	108 m	155 m	86 m	100 m	17 m	25 m	14 m	24 m
21	101 m	146 m	82 m	100 m	16 m	24 m	13 m	23 m
22	95 m	139 m	78 m	100 m	15 m	23 m	12 m	22 m
23	89 m	133 m	75 m	100 m	14 m	22 m	12 m	21 m
24	84 m	126 m	71 m	100 m	13 m	20 m	11 m	20 m
25	79 m	122 m	68 m	100 m	13 m	20 m	11 m	19 m
26	74 m	116 m	65 m	100 m	12 m	19 m	10 m	19 m
27	69 m	112 m	64 m	100 m	11 m	18 m	10 m	18 m
28	67 m	108 m	61 m	100 m	11 m	17 m	10 m	17 m

	AWG 16 (1.3 mm) Twisted-Pair Cable				AWG 24 (0.511 mm) Category 5 Cable			
	Bus Topology		Free Topology		Bus Topology		Free Topology	
PULs	AC	DC	AC	DC	AC	DC	AC	DC
29	62 m	104 m	59 m	100 m	10 m	17 m	9 m	16 m
30	59 m	99 m	57 m	99 m	9 m	16 m	9 m	16 m
31	57 m	96 m	55 m	96 m	9 m	16 m	9 m	16 m
32	52 m	92 m	52 m	92 m	8 m	15 m	8 m	15 m
Note: All distances assume a maximum average wire temperature of 55 ºC (130 ºF).								

Distributing the devices in a Pyxos FT network can increase the allowable distance of the devices from the power source. Use **Table 17**, and calculate your allowable distance according to the following formula:

$$\sum_{i=1}^{N}\left[\left(P_i\right)\times\left(d_i\right)\right]=const$$

where:

- N is the number of devices in the network
- P_i is the number of PULs for the ith device, placed distance d_i from the source power
- *const* is a constant value for the network

To use this formula, first consider all of your network's PULs located at a certain base distance from the source power, then distribute the PULs uniformly around that distance so that the average distance of all the PULs is the same as the base distance. For a bus-topology network, distribute the PULs along the bus; for a free topology network, distribute the PULs within a single branch of the network.

Example 1: Suppose that you have a network of 20 nodes in a bus-topology network, each requiring 40 mA of application current, and running link power from an AC source power supply on Category 5 wire. How far can the devices be from the source power? Because each device requires more than 35 mA of application current, you count 1 PUL for each device, for a total of 20 PULs in the network. Referring to **Table 17**, the average distance for 20 PULs (in a bus with an AC source power supply on Category 5 wire) is 17 m from the source power. Thus, if you ensure that the average distance for the 20 nodes from their source power is 17 m, then some of the 20 devices can be placed further from the source power. For example, if 10 of the devices are placed 14 m from the source, the other 10 devices can be placed up to 20 m from the source because the average distance remains 17 m (10 PUL at 14 m = 140 and 10 PUL at 20 m = 200; [140+200]/20 = 17), as shown in **Figure 27**. And because this network uses a bus topology, it is not limited by total wire length, that is, the bus length is well within the limit of 400 m total wire.

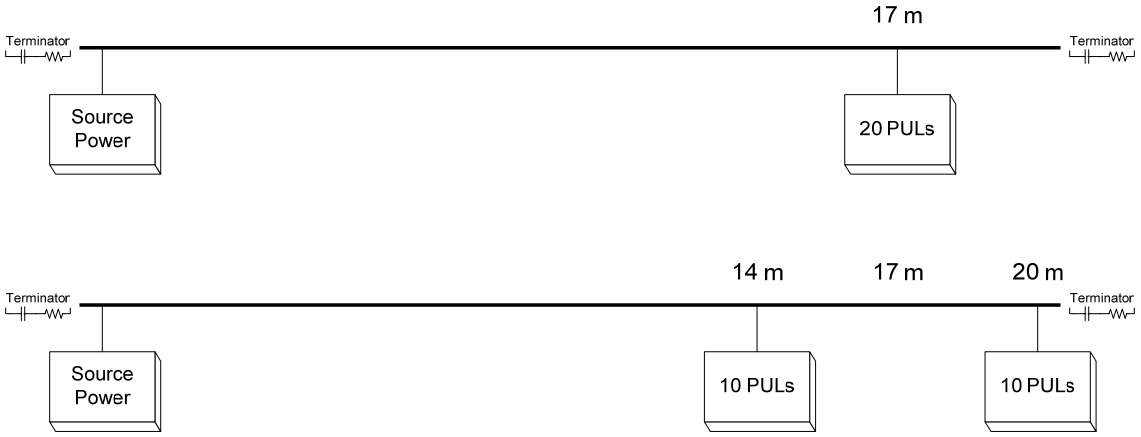

Figure 27. Example 1: Distributing PULs within a Bus Network

Example 2: Suppose that you have a network of 10 devices in a free-topology network, each requiring 20 mA of application current, and running link power from a DC source power supply on AWG 16 wire. How far can each device be from the source power? Because each device requires less than 35 mA of application current, you count ½ PUL for each device, which gives a total of 5 PULs for the 10 devices. Thus, referring to **Table 17**, the average distance for devices on any one network branch can be up to 100 m from the source power. In this case, your network is not limited by link power distance but by the total length of wire for a free topology Pyxos FT network, which can be no more than 100 m.

7

Design and Test for Electromagnetic Compatibility

This chapter describes electromagnetic compatibility design considerations for Pyxos FT devices and the tests that you perform to ensure immunity.

Overview

A product that is designed for electromagnetic compatibility (EMC) must be able to pass rigorous tests for immunity to external interference and demonstrate low electromagnetic interference (EMI) emissions. If the product will be sold in the European Union (EU), the product must demonstrate appropriate EMC levels to pass European Conformité Européene[4] (CE) Marking tests. Even if the product will not be sold in the EU, immunity testing helps you to design a better, more robust product.

Echelon has performed immunity tests for CE Marking on Pyxos FT devices, and has also performed additional tests to ensure immunity and low emissions. Specifically, Echelon has performed the following immunity tests:

- Electrostatic discharge (ESD) testing (both air and contact discharge) for compliance with International Electrotechnical Commission (IEC) standard 61000-4-2
- Radiated radio frequency (RF) immunity testing for compliance with IEC standard 61000-4-3
- Burst testing for compliance with IEC standard 61000-4-4
- Surge testing for compliance with IEC standard 61000-4-5
- Conducted RF Immunity testing for compliance with IEC standard 61000-4-6
- 50-60 Hz common-mode noise immunity testing
- Link power network shorting tests

Summary and Testing Results on page 73 summarizes the results of Echelon's testing for Pyxos FT devices.

You need to perform your own immunity testing for Pyxos FT devices that you design and build; however, you do not need to repeat the 50-60 Hz common-mode noise immunity testing or the link power network shorting tests.

The test results for each of the IEC standard 61000-4-x tests are interpreted within the scope of the product's specifications and standard operating conditions. A product's test results fall into one of the following categories, which are referred to as "performance criteria":

1. Normal product performance within specified limits
2. Temporary degradation or loss of function, or performance that is self-recoverable
3. Temporary degradation or loss of function, or performance that requires operator intervention to reset the system
4. Degradation or loss of function that is not recoverable

For example, within a Pyxos FT network, losing one network frame because of an ESD or surge hit likely meets category 1 because the Pyxos FT Chip resends network data that is not acknowledged as received. However, if your Pyxos FT application required absolute determinism, then losing a frame because of an ESD or surge hit would meet category 2.

For more information about the IEC standard tests and to purchase copies of the standards documents, go to the Information Handling Services (IHS) Global page: http://global.ihs.com. You can search for the EMC documents by selecting International Electrotechnical Commission (IEC) on the Standards page.

[4] European Conformity

Achieving High Immunity

Achieving immunity from ESD and other types of network transients requires good layout of the power, ground, and other device circuitry. In general, an ESD current will return to Earth ground or to other nearby metal structures. The device's ground scheme must be able to pass this ESD current between the network connection and the device's external ground connection without generating significant voltage gradients across the device.

To achieve high immunity, ensure that your design conforms to the following general guidelines:

- Use a star-ground configuration for your device layout
- Limit entry points in the device for ESD current
- Provide ground guarding for switching power supply control loops
- Provide good decoupling for V_{DD3} inputs
- Maintain separation between digital circuitry and cabling for the network and power

In a star-ground configuration, the power supply, network coupling circuit, and any I/O circuitry are distributed on the PCB in the form of a star, with the respective connectors and any chassis ground connections forming the center of the star. The host microprocessor and other sensitive circuitry should be as far from the center of the star as possible. The goal of the star-ground configuration is to conduct transients that enter the device on one cable out of the device through the other cables, with minimal disruption to other functional areas of the device. If the device has a metal chassis, ESD and other transients generally return to that chassis by way of the star-ground center point. If the device's logic ground is connected to this chassis ground, you should only connect it at this single point, with a short standoff, in the center of the star. Keep noisy digital lines (such as host microprocessor memory array lines) away from the metal enclosure walls. If a device is housed in a plastic enclosure and is powered with an isolating transformer, an explicit Earth ground or chassis ground might not be available. In this case, it is still important for the network connector and power supply connector to be located near the center of the star.

Switching power supply control loops can pick up radio-frequency (RF) noise and rectify it. RF immunity depends on limiting the pickup of such RF noise, so you need to provide sufficient ground guarding for the switching power supply control loops.

To provide good decoupling for V_{DD3} inputs, you should distribute V_{DD3} through low inductance traces and planes in the same manner as ground. All of the ground pins on the Pyxos FT Chip should be connected with either a ground plane (for PCBs with at least 4 layers) or a ground pad directly underneath the Pyxos FT Chip on the bottom of the board (for PCBs with 2 layers). Place one SMT decoupling capacitor per power pin between the Pyxos FT Chip and its host microprocessor (if any). Place each decoupling capacitor on the top side of the PCB, with the connection to its V_{DD3} pin as short as possible.

Maintaining separation between digital circuitry and cabling for the network and power limits RF crosstalk to any traces associated with the network or power supply (and any I/O lines that leave the device).

EMC Requirements for Deterministic Networks

The Pyxos FT Chip is designed to provide network determinism. However, if absolute determinism (that is, no lost data frames whatsoever) is important for a particular Pyxos FT application, you must design the overall system with extra care.

As described in the following sections, immunity tests, such as the ESD and surge tests, are generally considered to pass if only a frame or two are lost during the ESD or surge event, and the system continues to function normally after the transient. This is the normal definition for immunity to transients. According to the Pyxos FT protocol, the Pyxos FT Chip retries all missed messages, thus ensuring that no data is lost because of the transient event.

However, if absolute determinism is required for a particular application, then the loss of even a single frame would be unacceptable, even if the data is sent or received in the next frame. For these kinds of applications, extra physical design techniques are required to prevent these transients from getting onto the network and power wiring. For example, the network twisted pair cable could be concealed inside a conduit or within a metal enclosure. For link power system, it might be preferable to use battery backed DC link power (rather than AC link power), because the AC mains can experience intermittent outages that last days or weeks.

You can achieve absolute determinism with a Pyxos FT network, as long the design accommodates the requirements of the physical accessibility of the network and power wiring. In addition, there are some software considerations that apply to absolute determinism in networks. See the *Pyxos FT Programmer's Guide* for more information about software considerations for determinism.

Electrostatic Discharge

Electronic systems in industrial and commercial environments frequently encounter electrostatic discharge (ESD). An ESD event is a momentary electric current that flows between electrically charged objects at different voltage potentials (one of which can be ground). The most common form of ESD is an electric spark, but not all ESD hits are accompanied by a spark.

A reliable system design must consider the effects of ESD, and take steps to protect sensitive components. Static discharges occur frequently in low-humidity environments when human operators touch electronic equipment. Keyboards, connectors, and enclosures can also provide paths for static discharges to reach ESD-sensitive components. In addition, the European Community has adopted requirements for ESD testing.

There are two general approaches to minimizing the effects of ESD for an electronic product:

- Seal the product to prevent static discharges from reaching sensitive circuits inside the package.
- Design the grounding of the product so that ESD hits to user-accessible metal parts can be shunted around sensitive circuitry.

Because a Pyxos FT network connector is likely to be user-accessible, it is generally not possible to seal Pyxos FT devices completely. However, the product's package should be designed to minimize the possibility of an ESD hit arcing into the device's circuit board. If the product's package is made of plastic, then the PCB should be supported within the package so that unprotected circuitry on the PCB is not adjacent to any seams in the package. The PCB should not touch the plastic of an enclosure near a seam, because a static discharge can creep along the surface of the plastic, through the seam, and arc onto the PCB.

After an ESD hit arcs into the product, the current from the discharge flows through all possible paths back to Earth ground. The grounding of the PCB, and the protection of user-accessible circuitry, must allow these ESD return currents to flow back to Earth ground without disrupting normal circuit operation of the Pyxos FT Chip, its host microprocessor (if any), or other device circuitry. Generally, this means that you should ensure that the ESD currents are shunted to the center of a star ground configuration (as described in *Achieving*

High Immunity on page 65), and then out to the product's chassis or Earth ground connection. If the device floats with respect to Earth ground, the ESD current can return capacitively to Earth by the network wire, the power supply wires, and the PCB ground plane.

Testing for ESD to comply with the IEC 61000-4-2 ESD immunity test standard is performed on a metal test table using an ESD transient generator. Level 4 testing involves injecting up to ±8 kV contact discharges and up to ±15 kV air discharges into the product under test. Depending on the product design, you can inject the discharges at the network connector, power connector, or other user-accessible areas. During the test, the device should continue to operate normally, with occasional frame loss due to the ESD hits.

Electromagnetic Interference

The high-speed digital signals that are associated with microcontroller designs can generate unintentional electromagnetic interference (EMI). This interference is emitted by electrical circuits that carry rapidly changing signals that generate RF currents that can cause unwanted signals to be induced in other circuits. These unwanted signals can interrupt or degrade the effective performance of those other circuits.

Products that use a Pyxos FT Chip will generally need to demonstrate compliance with EMI limits enforced by various regulatory agencies. In the USA, the Federal Communications Commission (FCC) requires that industrial products comply with Title 47 of the Code of Federal Regulations (CFR) Part 15, Subpart A, and it requires that products which can be used in residential environments comply with Subpart B. The European comité européen de normalisation electrotechnique[5] (CENELEC) EN 55022 standard and the international comité international spécial des perturbations radioélectriques[6] (CISPR) 22 standard both require similar compliance, and most countries throughout the world require compliance with similar regulations.

A typical Pyxos FT device has several digital signals switching in the 10 MHz range. These signals generate voltage noise near the signal traces, and also generate current noise in the signal traces and power supply traces. The goal of good device design is to keep this voltage and current noise from coupling out of the product's package. Thus, careful PCB layout can ensure that a Pyxos FT device achieves the desired low level of EMI emissions.

It is important to minimize the leakage capacitance from circuit traces in the device to any external pieces of metal near the device, because this capacitance provides a path for the digital noise to couple out of the product's package. **Figure 28** on page 68 shows the leakage capacitances to Earth ground from a device's logic ground ($C_{leak,GND}$) and from a digital signal line in the device ($C_{leak,SIGNAL}$).

[5] European Committee for Electrotechnical Standardization

[6] International Special Committee on Radio Interference

Figure 28. Parasitic Leakage Capacitances to Earth Ground

If the Pyxos FT device is housed inside a metal chassis, that chassis likely has the largest leakage capacitance to other nearby pieces of metal. If the device is housed inside a plastic package, use PCB ground guarding to minimize $C_{leak,SIGNAL}$. Effective guarding of digital traces with logic ground reduces $C_{leak,SIGNAL}$ significantly, which reduces the level of common-mode RF currents driven onto the network cable.

For a device mounted near a piece of metal, especially metal that is Earth grounded, any leakage capacitance from fast signal lines to that external metal provides a path for RF currents to flow. When V_{gate} is pulled down to logic ground, the voltage of logic ground with respect to Earth ground increases slightly. When V_{gate} is pulled up to V_{DD3}, logic ground is pushed down slightly with respect to Earth ground.

As $C_{leak,SIGNAL}$ increases, a larger current flows during V_{gate} transitions, and more common-mode RF current couples onto the network twisted pair. This common-mode RF current can generate EMI in the 30-500 MHz frequency range, well in excess of CFR Part 15 Subpart B or CISPR 22 Level B levels, even when the capacitance of $C_{leak,SIGNAL}$ from a clock line to Earth ground is less than 1 pF. Thus, it is essential to guard clock lines for meeting Subpart B limits.

By using 0.1 µF or 0.01 µF decoupling capacitors at each digital IC power pin, you can reduce V_{DD3} and logic ground noise. You can then use logic ground as a ground shield for other noisy digital signals and clock lines.

For locally powered devices, some amount of filtering might also be required on a Pyxos FT device's power supply input, depending on the level of noise generated by the application circuitry. A good way to achieve this filtering is to place ferrite chokes in series with the power input traces adjacent to the power connector. **Figure 29** on page 69 shows a typical power supply circuit illustrating the placement of these ferrite chokes.

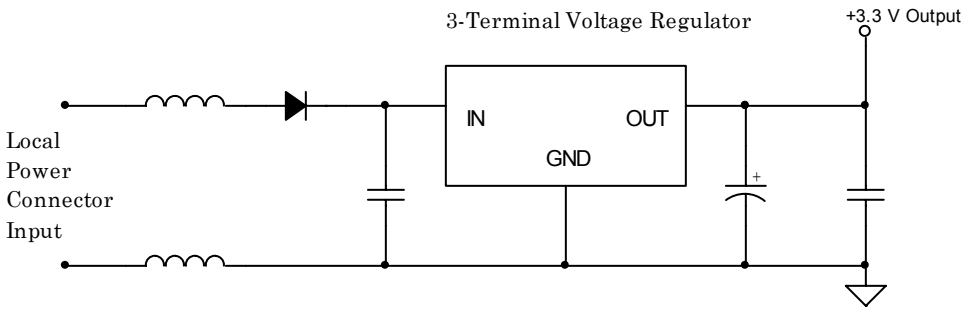

Figure 29. Power Supply Input Filtering Using Ferrite Chokes

Testing for EMI to comply with the CISPR 22 Radio Disturbance Characteristics test standard takes two forms:

- Radiated EMI testing checks for RF noise that radiates from network and power cables (or from inside the device)
- Conducted EMI testing checks for RF noise that radiates from the power supply connection to the AC mains

Compliance with the CISPR 22 Class A standard is required for industrial products, and compliance with the Class B standard is required for products that can be used in residential environments.

The following general rules and guidelines summarize EMI design considerations:

- The faster the clock speed for a Pyxos FT device, the higher the level of EMI.
- Better V_{DD3} decoupling quiets RF noise at the sources (the digital ICs), which lowers radiated EMI.
- A four-layer PCB generates less EMI than a two-layer PCB because the extra layers provide better V_{DD3} decoupling and more effective logic ground guarding.
- You can use a two-layer PCB for a Pyxos FT device and meet CFR Part 15 Subpart B or CISPR 22 Class B requirements if you include good decoupling and ground guarding.

Radiated and Conducted Immunity

The IEC 61000-4-3 RF Susceptibility and IEC 61000-4-6 Conducted RF Immunity tests ensure that a device's operation is not impaired by strong electromagnetic fields, such as those generated near cellular phones and portable radios.

The IEC 61000-4-3 RF Susceptibility test is generally performed in an RF-shielded anechoic chamber with high-power transmitter-driven antennas aimed at the EUT. During the IEC 61000-4-3 RF Susceptibility test, the RF signal generator is set to an AM depth of 80% at 1 kHz, and the frequency is slowly swept from 30 MHz to 1 GHz. With this condition, there are three levels of testing:

- Level 1, which represents a relatively well-insulated environment, subjects the EUT to a 1 V/m field strength
- Level 2, which represents a moderate electromagnetic radiation environment, subjects the EUT to a 3 V/m field strength
- Level 3, which represents a severe electromagnetic radiation environment, subjects the EUT to a 10 V/m field strength

During the IEC 61000-4-6 Conducted RF Immunity test, the RF signal generator is set to an amplitude modulation (AM) depth of 80% at 1 kHz, and the frequency is slowly swept from 150 kHz to 80 MHz. With this condition, there are three levels of testing:

- Level 1, which represents a relatively well-insulated environment, injects a common-mode voltage on the EUT's network cable of 1 V_{RMS} (5 V_{PP} including the 80% AM)
- Level 2, which represents a light industrial environment, injects a common-mode voltage on the EUT's network cable of 3 V_{RMS} (15.3 V_{PP} including the 80% AM)
- Level 3, which represents a harsh industrial environment, injects a common-mode voltage on the EUT's network cable of 10 V_{RMS} (50.9 V_{PP} including the 80% AM)

For twisted-pair networks, the preferred test method is the Current Injection method, also called the Bulk Current Injection (BCI) method. A current clamp injects common-mode noise onto the twisted-pair communication cable, and both the auxiliary equipment and the EUT experience similar common-mode noise at their network connections. Even when this wiring passes through a coupling-decoupling network, the RF noise that is present during the test can disrupt wired communication between the auxiliary equipment and an external control PC. Thus, the auxiliary equipment should provide a visual indication of a pass/fail result during the test, rather than requiring a wired connection to a computer to monitor the result.

Figure 30 shows a typical setup for IEC 61000-4-6 testing of a Pyxos FT device with unshielded twisted pair (UTP) network wire.

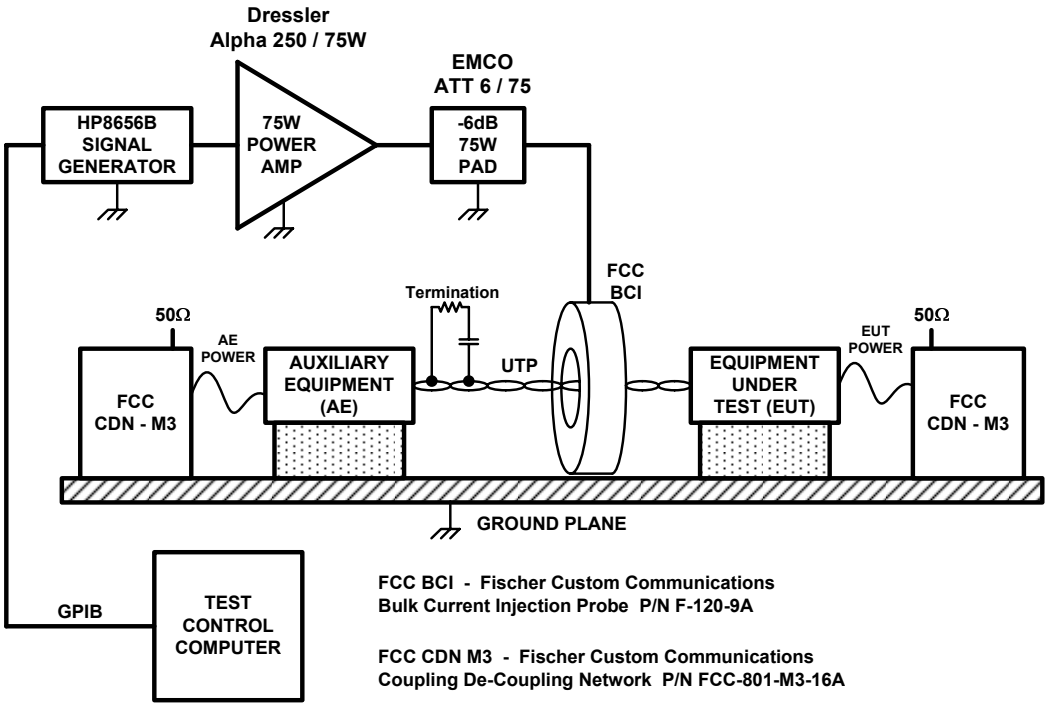

Figure 30. Typical IEC 61000-4-6 Test Setup for Unshielded Twisted Pair (UTP) Wire

For the IEC 61000-4-6 tests, the EUT is placed on a 10 cm high, non-conducting support on top of a metal ground plane. If the chassis of the EUT is connected to Earth ground in typical installations, for the test it should be connected directly to the metal ground plane with a short wire. If the EUT is left floating in normal use, there should be no connection between the EUT and Earth ground for the IEC 61000-4-6 tests.

Power connections for the auxiliary equipment and EUT should be routed through suitable decoupling devices, such as non-driven M3 CDNs. During the network immunity tests, any

I/O lines that come out of the auxiliary equipment or the EUT should also pass through a decoupling network. The objective of the BCI current clamp is to drive the large common-mode noise signal into the network cable of the EUT. The M3 CDNs ensure that the power supply inputs to the auxiliary equipment and EUT are not an RF return path.

For shielded twisted pair (STP) networks, the BCI current clamp injects common-mode noise into the STP cable. The cable shield should be connected to Earth ground with a parallel resistor and capacitor as shown in **Figure 31**. The resistor is generally 470 kΩ, 0.25 W, 5%. The capacitor is generally 0.1 µF, 10%, metal polyester, with a voltage rating of 100 VDC or higher.

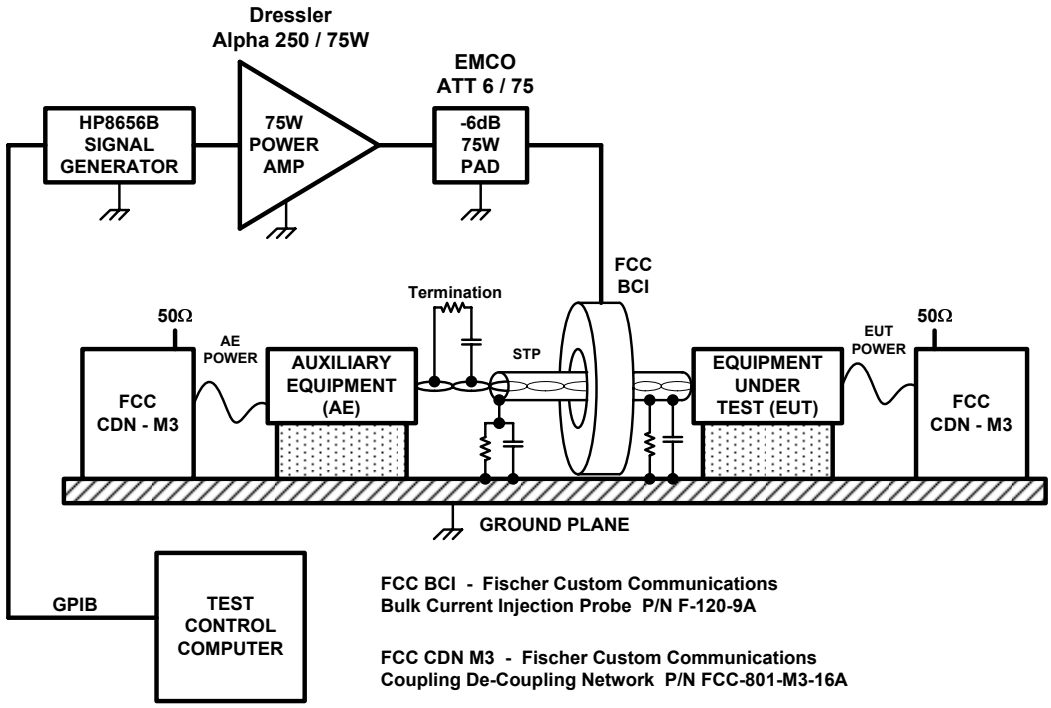

Figure 31. Typical IEC 61000-4-6 Test Setup for Shielded Twisted Pair (STP) Wire

For a Pyxos FT network, the overall immunity level that your device can achieve depends on the type of coupling circuit that you use for the device:

- Transformer-isolated coupling is the most robust
- Non-isolated coupling is somewhat less robust (but still better than an RS-485 network)
- A direct connection to the Pyxos FT network is the least robust

If the device is non-isolated (uses on-device grounding), floating the device's logic ground with respect to Earth ground can improve immunity.

See *Network Coupling Circuits* on page 37 for more information about coupling circuits.

Surge and Burst

For the purposes of EMC testing, a surge is a transient overvoltage of several kV with a rise time that is measured in microseconds or nanoseconds, and with a duration that is measured in microseconds. Compared with fast transient bursts and ESD, surges are relatively slow, but also long lived.

A surge is created by a switching event or insulation fault in the AC power distribution network, or by the switching of a reactive load (such as an electric motor). A surge can also be caused by lightning, but IEC 61000-4-5 only indirectly addresses the effects of lightning.

IEC 61000-4-5 Surge testing is performed on a non-conducting table using specialized surge generation equipment. The surges are injected directly into the network wiring (in a common-mode fashion) or into the power supply cable through a coupling circuit. During the test, the device should continue to operate normally, with occasional frame loss due to the surges.

There are three levels of network testing that are relevant to Pyxos FT devices:

- Level 2 conductively couples a ±1 kV surge into the network
- Level 3 conductively couples a ±2 kV surge into the network
- Level "X" conductively couples a user-defined surge voltage into the network

For link powered Pyxos FT networks that use 24 VAC source power with the AC line filter shown in **Figure 23** on page 55, the following differential Surge test levels have been verified:

- 2 kV Combo Wave with a source resistance of 2 Ω (per IEC 61000-4-5)
- 6 kV Combo Wave with a source resistance of 12 Ω (per IEC 61000-4-5)
- 6 kV Ring Wave with a source resistance of 12 Ω (per IEC 61000-4-12)

IEC 61000-4-4 Burst testing of the network cable is performed on a non-conducting table, with 1 meter of the network cable clamped in a high-voltage burst generation apparatus. The test capacitively injects high voltage bursts of noise into the network cable. The test injects three bursts onto the network cable each second. During the test, the device should continue to operate normally, with occasional frame loss due to the bursts.

There are two levels of network testing that are relevant to Pyxos FT devices:

- Level 3, which represents a typical industrial environment, injects ±1 kV bursts continuously for 60 seconds
- Level 4 which represents a severe industrial environment, injects ±2 kV bursts continuously for 60 seconds

In addition, burst testing is performed on the power supply input cable. For link powered Pyxos FT networks that use 24 VAC source power with the AC line filter shown in **Figure 23** on page 55, the following levels of power supply input testing are relevant to Pyxos FT devices:

- Level 3, which represents a typical industrial environment, injects ±2 kV bursts continuously for 60 seconds
- Level 4 which represents a severe industrial environment, injects ±4 kV bursts continuously for 60 seconds

Additional Testing

In addition to the IEC 61000-4-x tests, Echelon has tested the Pyxos FT Chip for DC to 60 Hz common-mode noise immunity and for link power network short immunity. Although you must repeat the IEC 61000-4-x tests for Pyxos FT devices that you design, you do not need to repeat these two tests.

DC to 60 Hz Common-Mode Noise Testing

This test drives common-mode noise onto the Pyxos FT network, and checks the integrity of communications on full-size networks for various Pyxos FT coupling options.

Link Power Network Shorting Testing

This test injects a momentary short (two harsh impulses) into a Pyxos FT link power network. The potential for each of the network twisted-pair wires is 24 V, and when the network is shorted, that short pushes a 24 V pulse into nearby Pyxos FT devices.

When the short is released, there is an inductive kickback effect that releases the energy that is stored in the shorted source power supply coupling inductance. The Pyxos FT devices that are near the source power supply need to be able to absorb this kickback energy.

The Pyxos FT Chip is designed so that it should sustain no damage from a link power network short.

Summary and Testing Results

Table 18 summarizes the results of the immunity and RF testing for a typical Pyxos FT application.

Table 18. Immunity and EMI Results

Test	Transformer-Isolated	Non-Isolated		Direct-Connect	
	Floating or Earth Grounded Device	Earth Grounded Device	Floating Device	Earth Grounded System	Floating System
IEC 61000-4-2 ESD	15 kV Air 8 kV Contact (Level 4)	15 kV Air 4 kV Contact [1] (Level 3)		15 kV Air 8 kV Contact (Level 4)	
IEC 61000-4-3 Radiated RF	10 V/m (Level 3)				
IEC 61000-4-4 Network Burst	2 kV (Level 4)				
IEC 61000-4-5 Network Surge	2 kV (Level 3)	N/A	2 kV (Level 3)	N/A	

Test	Transformer-Isolated	Non-Isolated		Direct-Connect	
	Floating or Earth Grounded Device	Earth Grounded Device	Floating Device	Earth Grounded System	Floating System
AC Link Power Differential Surge [2]	2 kV Combo Wave – source resistance 2 Ω 6 kV Combo Wave – source resistance 12 Ω 6 kV Ring Wave – source resistance 12 Ω			N/A	
IEC 61000-4-6 Conducted RF	10 V_{RMS} (Level 3)	1 V_{RMS} (Level 1)	3 V_{RMS} (Level 2) [3]	1 V_{RMS} (Level 1)	3 V_{RMS} (Level 2) [3]
Common-Mode Noise Immunity (DC to 60 Hz)	277 V_{RMS}	+/- 40 V (Peak)	Isolation Limit	0 V to V_{DD3}	Isolation Limit
Link Power Network Shorting	Pass			N/A	
CISPR 22 Radiated EMI	Level B				
CISPR 22 Conducted EMI	Level B				

Notes:

1. The IEC 61000-4-2 ESD test results for non-isolated coupling are preliminary.
2. This test applies to 24 VAC link-power networks that use the AC line filter shown in **Figure 23** on page 55.
3. The -6 immunity level for floating devices might be higher, depending on how well they are isolated from Earth ground.

8

Handling and Manufacturing

This chapter describes guidelines for handling and manufacturing devices that use the Pyxos FT Chip, including soldering profiles and ESD handling guidelines.

Recommended Solder Profile

Follow the general guidelines described in IPC/JEDEC Standard J-STD-020C when soldering Pyxos FT Chips to PCBs. This standard includes information for classification reflow profiles. The Pyxos FT Chip complies with the European Union Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC), thus its profile uses the lead-free assembly, with a peak temperature T_p of 260 °C, as summarized in **Table 19**.

Table 19. Peak Temperatures for Surface Mount Parts

Product	RoHS Compliant	Model Number	Peak Temperature
Pyxos FT Chip	Yes	11500R	260 °C
Note: The Pyxos FT Chip is available in two quantities, 300 (model number 11500R-300) and 5000 (model number 11500R-5000).			

As measured according to the IPC/JEDEC Standard J-STD-020C, the Pyxos FT Chip has a Level 3 Classification. The recommended soldering technique for Pyxos FT Chips is surface mount reflow. Soldering techniques that involve immersing the entire part are not recommended. Consult the solder manufacturer's datasheet for recommendations on optimum reflow profile.

Dry pack is a process that slowly bakes moisture from the surface mount technology package and seals it into a dry pack bag to shield the unit from moisture in the atmosphere. The exterior of the bag is marked with a label that indicates that the devices are moisture sensitive and is marked with the date that the bag was sealed (there is a one year shelf life for such devices).

There is a limited amount of time to use surface-mount devices after they are removed from the dry pack. Before surface mounting, packages should not be out of the dry pack longer than 168 hours at ≤ 60% relative humidity and ≤ 30 °C. If the units have not been shipped dry pack or have been unpacked for too long, then units must be baked at 125 °C for 12 hours prior to board soldering. If this is not done, some percentage of the units can exhibit destructive failures or latent failures after the soldering process.

ESD Handling Guidelines

All complementary metal-oxide-semiconductor (CMOS) devices have an insulated gate that is subject to voltage breakdown. The gate oxide for the Pyxos FT Chip breaks down at a gate-source potential of about 10 V. The high-impedance gates on the chip are protected by on-chip networks. However, these on-chip networks do not make the chip immune to ESD. Laboratory tests show that devices can fail after one very high voltage discharge. They can also fail due to the cumulative effect of several discharges of lower potential.

Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is shorted to V_{DD3}, shorted to GND, or is open-circuited. As a result of this damage, the device no longer functions. Less severe cases are more difficult to detect because they appear as intermittent failures or as degraded performance. Static damage can often increase leakage currents.

CMOS devices are not immune to large static voltage discharges that can be generated during handling. For example, static voltages generated by a person walking across a waxed

floor have been measured in the 4 kV – 15 kV range (depending on humidity, surface conditions, and so on). Therefore, you should observe the following general precautions:

1. Do not exceed the maximum ratings specified in the data sheet.
2. All unused device inputs should be connected to V_{DD3} or GND.
3. All low-impedance equipment (for example, pulse generators) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS devices is merely an extension of the device, and the same handling precautions apply. Contacting connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and is brought into contact with static-generating materials.
5. All CMOS devices should be stored or transported in materials that are antistatic. Devices must not be inserted into conventional plastic "snow," Styrofoam®, or plastic trays. Devices should be left in their original container until ready for use.
6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, because a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See **Figure 32** on page 78.
7. Nylon or other static-generating materials should not come in contact with CMOS circuits.
8. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines that come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material, or soldered onto a PCB.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following precautions apply during wave-solder operations:
    a. The solder pot and conductive conveyor system of the wave-soldering machine must be grounded to an Earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an Earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.

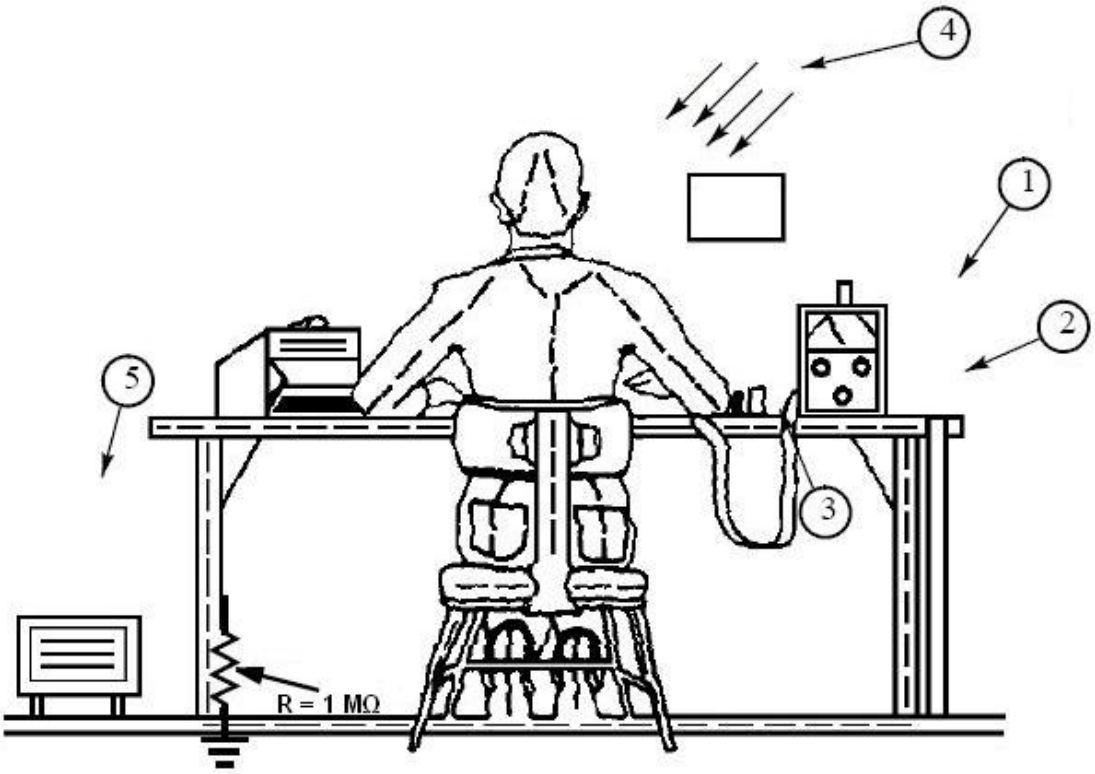

Figure 32. Typical Manufacturing Work Station

Notes for **Figure 32**:

1. 1/16 inch conductive sheet stock covering bench-top work area.
4. Ground strap.
5. Wrist strap in contact with skin.
6. Static neutralizer (ionized air blower directed at work). Primarily for use in areas where direct grounding is impractical.
7. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air, which causes the relative humidity inside a building to be less than outside humidity.

The following steps should be observed during board cleaning operation:

1. Vapor degreasers and baskets must be grounded to an Earth ground. Operators must likewise be grounded.
2. Brush or spray cleaning should not be used.
3. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
4. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
5. High-velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module. The use of static-detection meters for line surveillance is highly recommended.

6. The use of static-detection meters for line surveillance is highly recommended.
7. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
8. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
9. Double-check the equipment setup for proper polarity of voltage before conducting parametric or functional testing.
10. Do not reuse shipping rails. Continuous use causes deterioration of their antistatic coating.
11. Wrist straps and equipment logs should be maintained and audited on a regular basis. Wrist straps can malfunction and the malfunction can go unnoticed. Also, equipment is moved from time to time and grounds may not be reconnected properly.

A

Checklists

This appendix includes a set of checklists, including chip connections, coupling circuits, power supplies, PCB layout, and network cabling. These checklists help you ensure that products that you design for the Pyxos FT Chip meet the specifications described in this manual.

You can copy and freely distribute the contents of this appendix.

Checklist 1: Pyxos FT Chip Connections

Check When Complete	Item	Description
	CH1	There are at least two V_{DD3} decoupling capacitors for the Pyxos FT Chip. Each is placed directly adjacent to a V_{DD3} pin on the chip, on the top layer of the PCB, with a short connection to ground.
	CH2	The Pyxos FT Chip VBIAS pin has a 0.1 µF decoupling capacitor to ground, placed on the top layer of the PCB directly adjacent to the VBIAS pin.
	CH3	The Pyxos FT Chip RST~ pin has decoupling capacitors to V_{DD3} and ground, if necessary for ESD immunity (determined by ESD testing). See *The Reset Pin* on page 23 for more information about the RST~ pin.
	CH4	The JOIN/MD pin has the correct external circuitry to indicate to the Pyxos FT Chip whether the device is hosted or unhosted, as described in *Specifying Hosted or Unhosted Operating Mode* on page 26.
	CH5	The crystal oscillator connected to the Pyxos FT Chip XIN and XOUT pins is 10 MHz, 18 pF parallel resonant, and meets the accuracy requirements described in *Pyxos FT Chip Clock* on page 24.
	CH6	The Pyxos FT Chip XIN and XOUT pads and traces match the PCB layout rules for either 2-layer or 4-layer PCBs described in *Design Considerations for the Pyxos FT Chip Clock* on page 33.
	CH7	The PCB layer stackup of your board matches either the 2-layer or 4-layer PCB stackup described in *Design Considerations for the Pyxos FT Chip Clock* on page 33.
	CH8	On a blank PCB, when you measure the capacitance from the Pyxos FT Chip XIN pin to ground, you measure 3.5 pF ± 0.3 pF.
	CH9	On a blank PCB, when you measure the capacitance from the Pyxos FT Chip XOUT pin to ground, you measure 3.5 pF ± 0.3 pF.
	CH10	A 10.5 kΩ pullup resistor is connected between the Pyxos FT Chip XOUT pin and V_{DD3}.
	CH11	Other than the Pyxos FT Chip, the crystal oscillator, and the pullup resistor, there are no other connections to the Pyxos FT Chip XIN or XOUT pins.

Check When Complete	Item	Description
	CH12	For an unhosted device, unused I/Os are tied off to either V_{DD3} or ground (a resistor tie is optional).
	CH13	For a hosted device, the SPI clock signal SCLK has a 49.9 Ω "back termination" resistor placed directly adjacent to the host microprocessor's SCLK output pin.
	CH14	If the Pyxos FT Chip's COUT clock output is routed to another device on the PCB, a 49.9 Ω "back termination" resistor is placed directly adjacent to the Pyxos FT Chip, in series with that connection.

Checklist 2: Pyxos FT Device Coupling Circuit

Check When Complete	Item	Description
	CC1	If the device uses a direct connection to the Pyxos FT network, then all other devices on the network do as well, and they all share a common ground connection and common power supply.
	CC2	If the device uses non-isolated or floating topology, then the two inductors and two capacitors connected to the Pyxos FT Chip NET_A and NET_B pins meet the specifications listed for them in *Network Coupling Circuits* on page 37.
	CC3	If the device uses transformer-isolated topology, then the coupling capacitors and PCB spark gaps meet the specifications listed for them in *Network Coupling Circuits* on page 37, and the coupling transformer is the one specified (Transtek TMS80040CS).

Checklist 3: Pyxos FT Device Power Supply – General (Non-Link-Power)

Check When Complete	Item	Description
	PS1	V_{DD3} = 3.3V ± 10% over the full device temperature range and device application current range (including any ripple).
	PS2	Any ripple on V_{DD3} is ≤ 50 mV_{p-p}, measured with a 20 MHz bandwidth.
	PS3	The rise time of V_{DD3} at power-up meets the requirements of the host microprocessor (see the appropriate host microprocessor data sheet – the maximum allowable risetime is often listed).

Checklist 4: Pyxos FT Power Supply – Link Power Network

Check When Complete	Item	Description
	PN1	For AC link power, you have placed the Schaffner Line Filter (FS23488-3-06) between the AC mains supply and your 24 VAC source power transformer.
	PN2	For AC link power, you have verified that your 24 VAC source power transformer has the required 950 µH leakage inductance, measured directly or by using the procedure described in *Testing Transformer Leakage Inductance* on page 56.
	PN3	For AC link power, your 24 VAC source power transformer is rated for at least 55 VA, or has been scaled down according to the guidelines described in *AC Source Power* on page 55.
	PN4	For DC link power, you have verified that when connected as shown in **Figure 24** on page 56, the output noise at the DC source power supply output terminals (to the left of the inductors) is ≤240 mV_{p-p} when measured with a 20 MHz bandwidth.
	PN5	For DC link power, the DC source power supply output is rated for 24 VDC ± 10%, for up to 2.1 amps, or has been scaled down according to the guidelines described in *DC Source Power* on page 55.
	PN6	For DC link power, you use the filter circuit shown in **Figure 24** described in *DC Source Power* on page 55.

Checklist 5: Pyxos FT Power Supply – Link Powered Devices

Check When Complete	Item	Description
	LP1	Your device uses one of the link power node power supply reference designs described in Appendix B, *Reference Designs*, on page 91.
	LP2	For the DC-DC converter reference design, your application current is ≤ 100 mA, not including the current used by the Pyxos FT Chip.
	LP3	For the linear power supply reference design, your application current is ≤ 15 mA, not including the current used by the Pyxos FT Chip.

Checklist 6: Pyxos FT Device PCB Layout

Check When Complete	Item	Description
	LO1	Your design incorporates a "star ground" layout design, with the Pyxos FT network connector, coupling circuit, power supply input, and externally-accessible I/Os all grouped near each other along one edge (or two adjacent edges) of the PCB.
	LO2	If your device has a metal enclosure, the enclosure is tied to the center of the star ground through a low inductance connection (optionally with a low-inductance DC blocking capacitor in series).
	LO3	For 4-layer PCBs, the internal ground plane is used to connect the center of the star ground out to the ground connections of the other functional blocks. For 2-layer PCBs, ground pours on the bottom and top layers are used to connect the center of the star ground out to the ground connections of the other functional blocks.
	LO4	For transformer-isolated network coupling, there are spark gaps on the NET1 and NET2 connections, between the network connector and the communication transformer: • The spark gaps have the correct dimensions as shown in **Figure 19** on page 45, resulting in an 18 mil (0.46 mm) air gap. • The board finish for the outer layer exposed pads of the spark gap have immersion silver plating, such as Enthone AlphaSTAR immersion silver, with a 9 to 15 microinch (229 to 381 nm) finished thickness.
	LO5	For transformer-isolated network coupling, the ESD keepout area shown in **Figure 18** on page 43 has no traces or planes in the area shown, except for the connections from the NET1 and NET2 traces through the coupling capacitors and into the communication transformer.
	LO6	There is a low-inductance ground path from the Pyxos FT Chip back to the center of the star ground, to ensure that ESD and surge transients clamped inside the Pyxos FT Chip have a good return path back off of the PCB without going through any sensitive circuitry.
	LO7	If the device has a host microprocessor or any other digital circuitry that could generate RF noise, that circuitry is kept away from the network cable, power cable, and any I/O cables.

Checklist 7: Pyxos FT Network Cabling and Termination

Check When Complete	Item	Description
	NC1	Your Pyxos FT network uses one of the approved wire types described in *Network Cabling* on page 48.
	NC2	If absolute determinism is a requirement for the network, ensure that the network twisted pair cable is concealed inside conduit or within a metal enclosure. See *EMC Requirements for Deterministic Networks* on page 65 for more information about the requirements for determinism.
	NC3	For a free-topology Pyxos FT network, it uses the termination shown in **Figure 20** on page 49. For a bus-topology Pyxos FT network, it uses the two terminators shown in **Figure 21** on page 50.

B

Reference Designs

This appendix describes the reference designs for the node power supply that is required for a link-powered Pyxos FT device.

Important: The information provided in this appendix is preliminary and will be updated through the service process. See the Echelon documentation Web site (www.echelon.com/pyxos) for the most current information.

Linear Power Supply

Figure 33 on page 93 shows the circuit schematic for the linear power supply. **Table 21** on page 94 lists the parts needed for this circuit. **Figure 34** through **Figure 37** starting on page 95 show an example two-layer PCB layout for the linear power supply, as implemented for the Pyxos FT EVK EV-Nano Point evaluation board. The EV-Nano Point has a larger value for the current limit resistor R202, but its power supply circuit is otherwise the same as shown in the schematic.

The Linear Power Supply circuit uses the series pass transistor Q201 to drop the input voltage down to 3.3 V. The TL431 2.5 V voltage reference U202 compares a divided-down version of the output 3.3 V, and adjusts the base current to Q201 to keep the output voltage in regulation. This circuit provides up to 15 mA of application current, in addition to the current required for the receive and transmit operations of the Pyxos FT Chip.

The input diode bridge D201 rectifies the AC link power input waveform (or provides polarity insensitivity for DC link power). R202 and transistors Q202A/B provide a short-duration short-circuit protection feature to avoid overloading the link power network due to a V_{DD3} short at the power supply output. The current limit is approximately 100 mA, however, so an extended V_{DD3} short to ground can cause the linear power supply to fail.

Table 20 summarizes the basic characteristics of this design.

Table 20. Characteristics of the Linear Node Power Supply Design

Parameter	Value
Input Voltage Range	8.5 V to 40 V
Output Voltage	3.3 V ± 10%
Maximum Application Current	15 mA

Figure 34 and **Figure 35** show the top and bottom composite PCB layout plots; **Figure 36** and **Figure 37** show just the top and bottom metal layers of this two-layer PCB. The network connector JP102 is at the upper right, and the Linear Power Supply circuitry is in the upper left area of the PCB.

Note the use of the two-sided PCB metal island that provides the heat sink area for Q201 in the upper left of the PCB. A metal island is formed on the top and bottom layers, and stitched through with vias. This island is not at ground potential, because it is connected to the collector of Q201

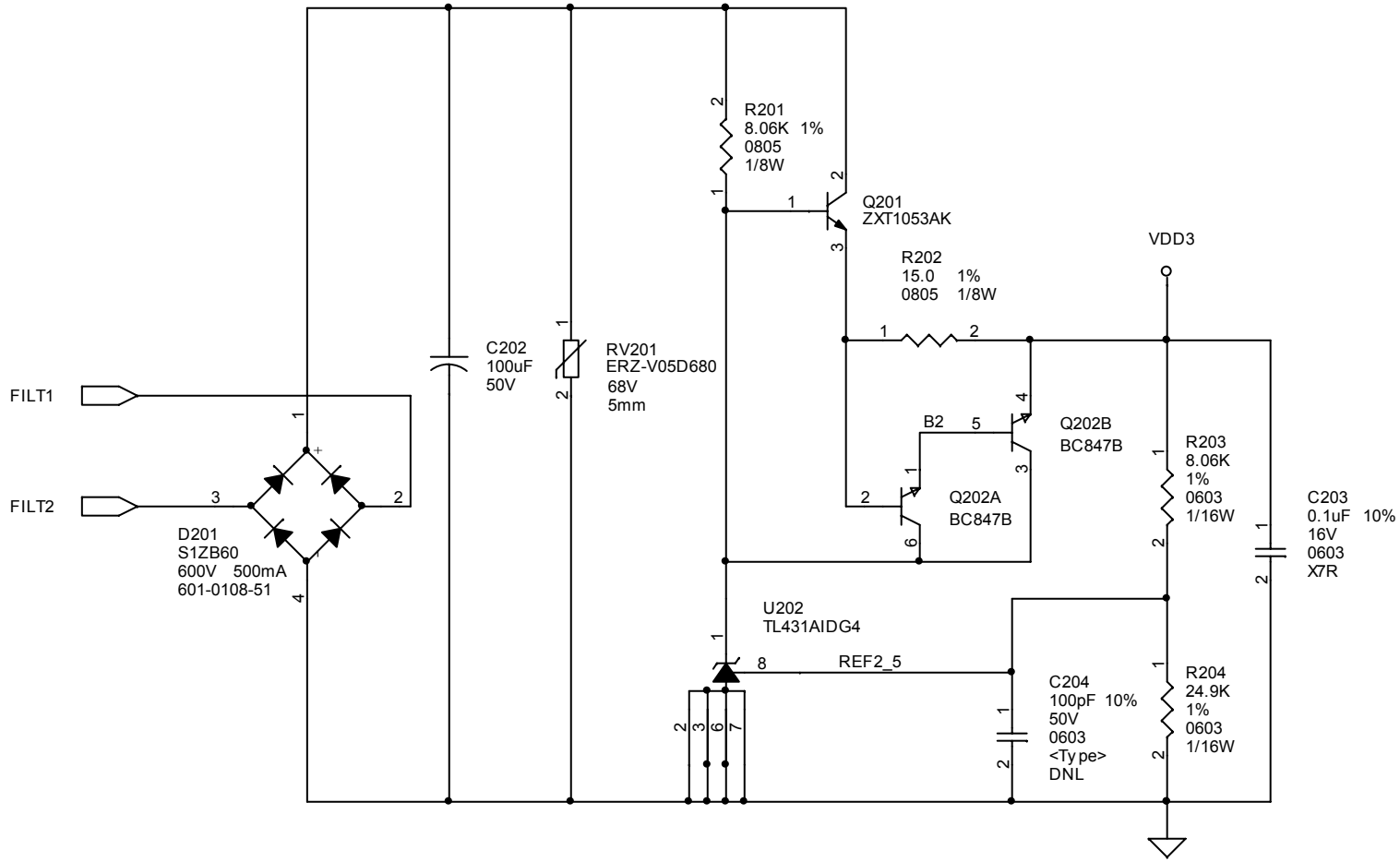

Figure 33. Linear Power Supply Schematic

Table 21. Parts for Linear Power Supply

Part	Value	Required Specifications	Example Vendor Part Number
C202	100 µF	±5% ≥ 50 VDC	Nichicon UHE1H101MPD
C203	0.1 µF	10% ≥ 16 V	Kemet C0603C104K3RACTU
C204	100 pF	10% ≥ 50 V	Murata GRM1885C1H101JA01D
D201	Bridge	600V ≥ 500 mA	Shindengen S1ZB60-7062
Q201		NPN transistor ≥ 75 V, ≥ 5 A	Zetex ZXT1053AKTC PB-FREE
Q202A (dual)		NPN transistors	ON Semiconductor BC847BDW1T1G
R201	8.06 kΩ	1% ≥ 1/8 W	KOA Speer RK73H2ATTD8061F
R202	15.0 Ω	1% ≥ 1/8 W	Yageo 232273461509L
R203	8.06 kΩ	1% ≥ 1/16 W	Panasonic ERJ-3EKF8061V LEADFREE
R204	24.9 kΩ	1% ≥ 1/16 W	Yageo RC0603FR-0724K9L
RV201	MOV	68 V Varistor 5 mm	Panasonic ERZ-V05D680 LEADFREE
U202		2.5 V shunt regulator	Texas Instruments TL431IDBVRE4

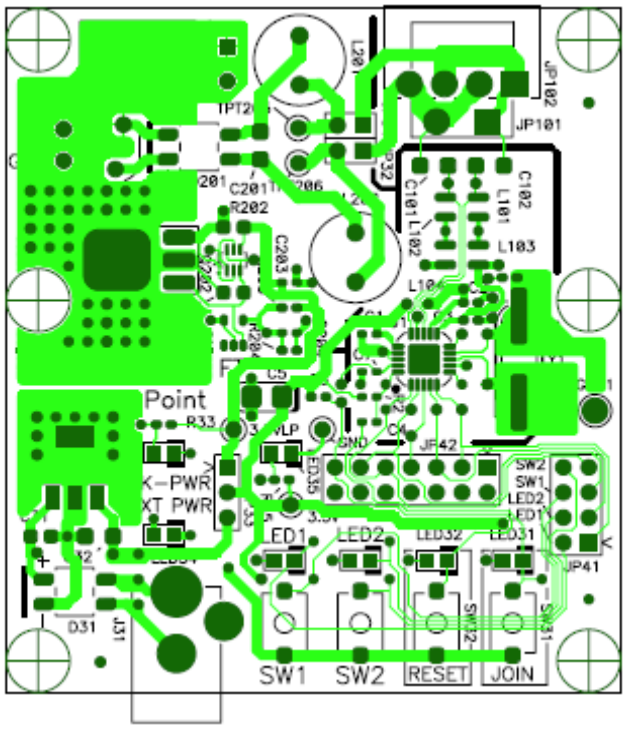

Figure 34. Top Layer Composite Layout of EV-Nano Point with Linear Power Supply

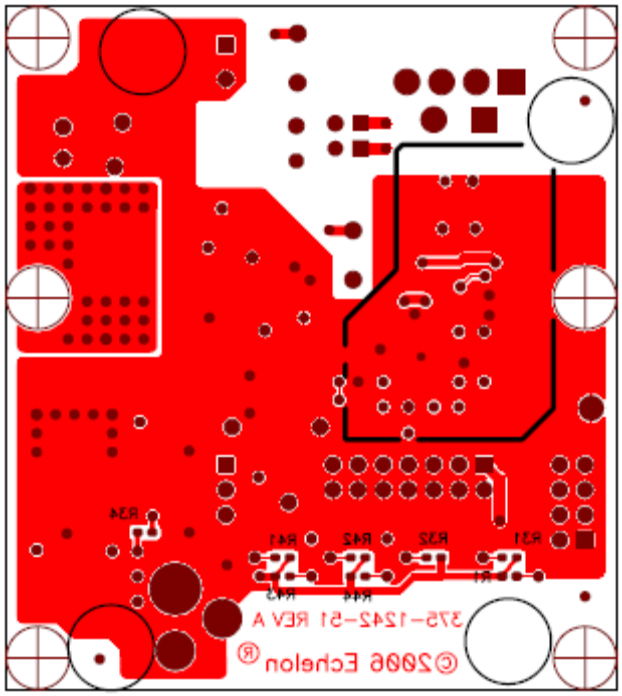

Figure 35. Bottom Layer Composite Layout of EV-Nano Point with Linear Power Supply

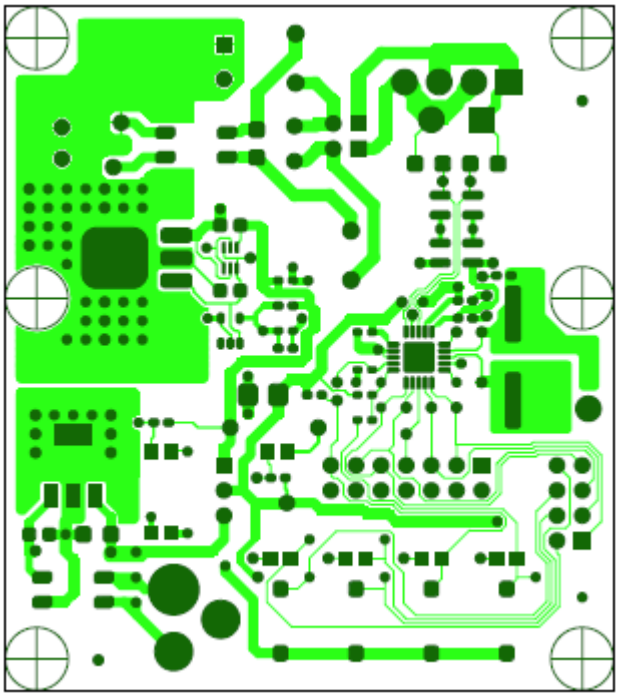

Figure 36. Top Metal Layer of EV-Nano Point with Linear Power Supply

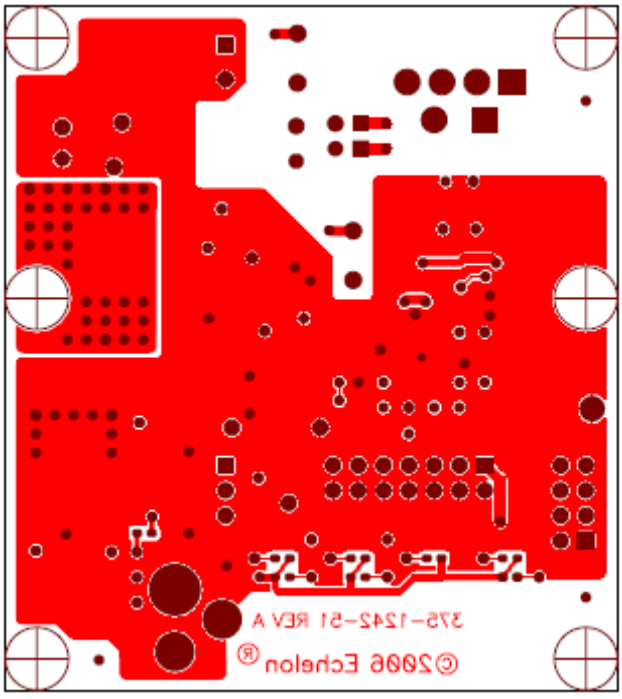

Figure 37. Bottom Metal Layer of Nano Point with Linear Power Supply

Switching Power Supply

Figure 38 on page 98 shows the circuit schematic for the switching power supply.

The switching power supply circuit uses transistor Q201, transformer T201, and diode D201 to step down the input voltage to provide the 3.3 V output. This circuit provides up to 100 mA of application current, in addition to the current required for the receive and transmit operations of the Pyxos FT Chip.

The input diode bridge D201 rectifies the AC link power input waveform (or provides polarity insensitivity for DC link power). This switching power supply circuit uses a discrete "blocking oscillator" or "ringing choke circuit" (RCC) design. This discrete approach can provide significant cost savings, as compared to a design using off-the-shelf switching regulator control ICs. The third winding on the transformer (pins 2-5) is part of this self-oscillating circuit.

Feedback for regulation is provided by the TLV431 1.25 V voltage reference U202 and optocoupler U201. The switching frequency varies with the output loading on V_{DD3}. The switching frequency varies from approximately 50 kHz at full load to approximately 150 kHz at light loads. At light loads, some burst operation occurs, but this has no effect on the integrity of the Pyxos FT communications.

This circuit is fully protected against output short circuits on the V_{DD3} rail, and the output recovers smoothly back to 3.3 V when the output short is removed.

Table 22 summarizes the basic characteristics of this design.

Table 22. Characteristics of the Switching Node Power Supply Design

Parameter	Value
Input Voltage Range	8.5 V to 40 V
Output Voltage	3.3 V ± 10%
Maximum Application Current	100 mA

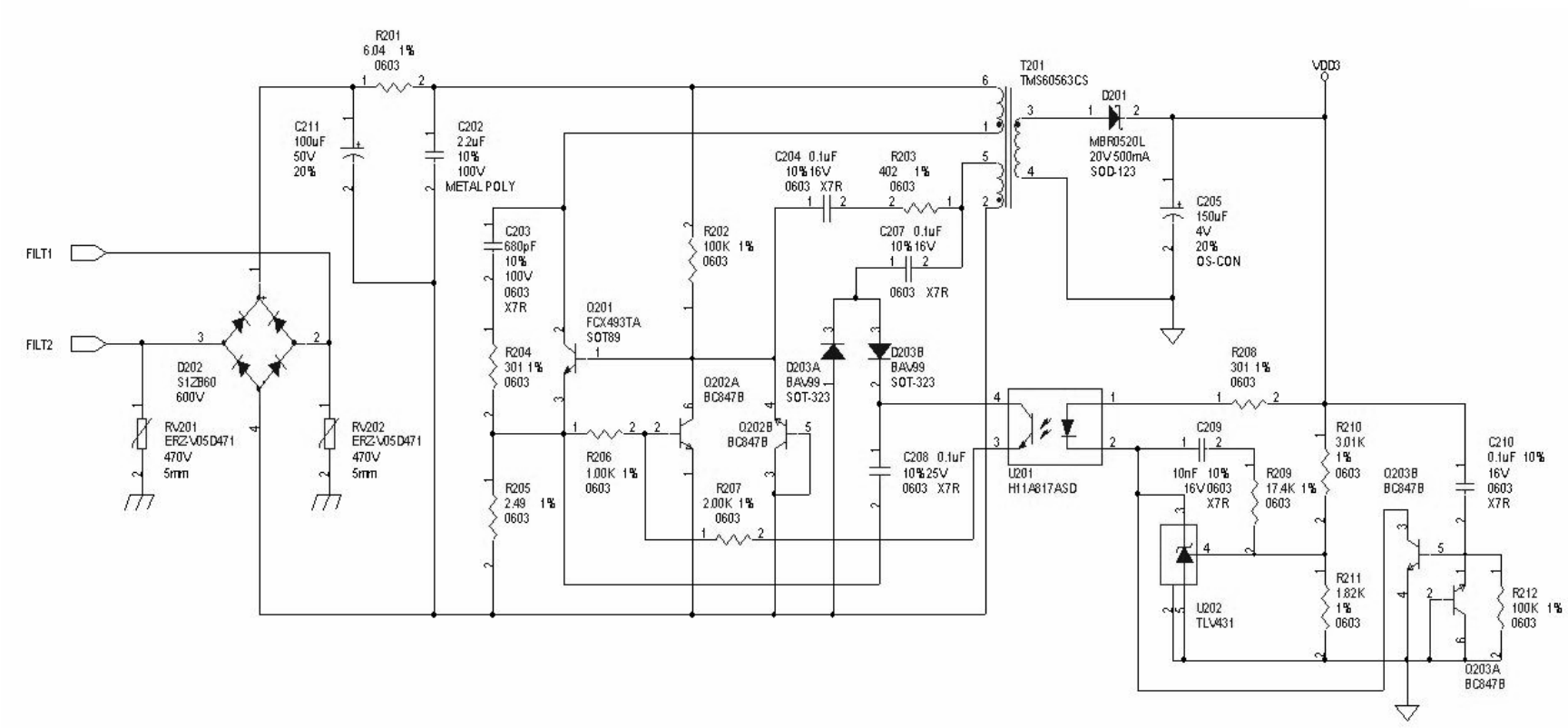

Figure 38. Switching Power Supply Preliminary Schematic

Detailed information for the switching power supply, including an updated circuit schematic, parts list, and layout diagram will be provided through the service process. See the Echelon Pyxos Web site (www.echelon.com/pyxos) for the most current information.

C

Vendor Contact Information

This appendix lists contact information for many of the product vendors mentioned in this manual.

Vendor Information

This appendix lists contact information for many of the product vendors mentioned in this manual. This information was current as of the publication of this manual. For most of the parts listed in this manual, Echelon does not require that you use these vendors, but has tested the Pyxos FT Chip with products from the vendors listed.

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